The Dynamics of Latchup Turn-On Behavior in Scaled CMOS

SHINJI ODANAKA, MUTSUKO WAKABAYASHI, AND TAKASHI OHZONE

Abstract—This paper presents the dynamics of latchup turn-on behavior in scaled CMOS structures using an exact time-dependent and two-dimensional numerical analysis based on the finite-difference approach. Both the dynamics of surface-induced latchup triggering by a parasitic PMOSFET and direct forward biasing are examined to discuss the two-dimensional effects of parasitic devices in a scaled CMOS structure during latchup turn-on. In the case of an n-well scaled CMOS, the two-dimensional nature of the well structure plays an important role for surface-induced latchup.

I. Introduction

THE DEVELOPMENT of CMOS integrated circuits has become of major interest in VLSI technology. Latchup phenomena, however, limit the densities of CMOS. In high-density CMOS circuits, it becomes difficult to determine how to scale down CMOS structures and layout rules of CMOS circuits without understanding latchup turn-on mechanisms.

In particular, several authors have paid much attention to the dynamics of latchup turn-on for achieving high latchup immunity of CMOS circuits [1], [2]. Although they have investigated the dynamics of latchup turn-on based on their proposed analytical models, these models did not include the multidimensional effects of current flow paths and the resistances depending on parasitic device geometries. More recently, G. J. Hu has been the first to show that two-dimensional transient analysis is more effective in explaining the entire CMOS latchup turn-on process [3], [4]. He has also pointed out that the latchup holding voltage is a meaningful term for the evaluation of latchup immunity based on simulated results. Although two-dimensional transient analysis is required for much CPU time, it can be used for showing quantitative characteristics of parasitic devices in a CMOS structure during latchup turn-on.

In this paper, the dynamics of latchup turn-on behavior are examined using an exact time-dependent and two-dimensional device simulator. The two-dimensional effects of parasitic devices in a scaled non-epi CMOS structure during latchup turn-on are discussed for achieving the optimum scaling of a CMOS structure. For this purpose, in particular, the study of so-called surface-induced latchup, as D. Tacaks *et al.* pointed out [5], is focused on. In reducing lateral dimensions of a CMOS structure, it is shown that the two-dimensional nature of the well structure as well as the influence of a parasitic wiring line over the field oxide plays an important role for surface-induced latchup. In the case of an n-well CMOS process, the two-dimensional action of the parasitic p-n-p transistor leads to the decrease of latchup immunity of the CMOS structure.

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II. Brief Description of the Two-Dimensional Numerical Device Simulator

A. Device Model

The latchup turn-on behaviors of n-well CMOS structures are investigated using the results of a two-dimensional numerical device simulator. This simulator has been developed to obtain transient solutions of Poisson's equation and continuity equations for electrons and holes in a two-dimensional cross section of nonplanar semiconductor devices such as CMOS structures.

Under nondegenerate conditions, the electron and hole diffusion coefficients D_n, D_p and the mobilities μ_n, μ_p are related by Einstein relation, and carrier densities are given by the Boltzmann approximation. The device is modeled by Poisson's equation and current continuity equations.

$$\epsilon_s \nabla^2 \psi = -q(N - n + p) \tag{1}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla J_n - R \tag{2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla J_p - R. \tag{3}$$

The continuity equations (2) and (3) are further specified by writing the current density J_n and J_p in the following forms:

$$J_n = -q\mu_n n \nabla \psi + qD_n \nabla n \tag{4}$$

$$J_p = -q\mu_p p \nabla \psi - qD_p \nabla p \tag{5}$$

where $N = N_D^+ - N_A^-$ is the active impurity concentration and n and p are the electron and hole densities, respectively. ψ is the electrostatic potential. q is the electronic charge, and ϵ_s is the semiconductor permittivity. In this work, the displacement current is neglected.

The boundary conditions for the electrostatic potential ψ satisfy the following forms:

$$\psi = V \pm \frac{kT}{q} \ln (|N|/n_i) \tag{6}$$

at the n^+ or p^+ contacts and

$$\nabla \psi \cdot \hat{n} = 0 \tag{7}$$

at boundaries except for the n^+ and p^+ contacts. For the continuity equations, the electron and hole densities are set up to be

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the value of the doping concentration at the n^+ or p^+ contacts, respectively. At the boundaries except for the n^+ and p^+ contacts, the current densities normal to the boundary lines are zero; $J \cdot \hat{n} = 0$, where V is an applied voltage. $\hat{n}$ is the unit vector normal to the boundaries. n_i is the intrinsic carrier density. k is Boltzmann's constant and T is the carrier temperature.

The factor R is introduced as the bulk and surface Schockley-Read-Hall recombination processes and Auger recombination process [6], [7]. In this work, the avalanche generation term and bandgap narrowing effects are neglected.

$$R_{SRH} = (n_i^2 - pn)/[\tau_n(p + n_i) + \tau_p(n + n_i)] \tag{8}$$

$$R_{SUR} = \delta(y - y_s)\,(n_i^2 - pn)/[(p + n_i)/s_n + (n + n_i)/s_p] \tag{9}$$

$$R_{AUG} = (n_i^2 - pn)\,(C_n \cdot n + C_p \cdot p) \tag{10}$$

where τ_n and τ_p are the electron and hole lifetimes, 1.1×10^{-6} s, 3.5×10^{-7} s, respectively. s_n and s_p are the surface recombination velocities. C_n and C_p are Auger recombination coefficients. $y = y_s$ denotes the SiO_2-Si interface. δ is the Dirac delta function. It is assumed the most effective trap occurs in the middle of the bandgap.

The electron and hole mobilities μ_n and μ_p are modeled in the following form [8]:

$$\mu(N, E) = \frac{\mu_0(N)}{\left[1 + \left(\dfrac{\mu_0(N) \cdot E}{v_{sat}}\right)^2\right]^{1/2}} \tag{11}$$

where $\mu_0(N)$ is the low field mobility and v_{sat} is the saturation velocity. E is the electric field.

The two-dimensional doping profile is calculated by the one-dimensional process simulator SUPREM-II [9], which is fitted in the lateral directions.

B. Discretization

The three coupled nonlinear partial differential equations (1), (2), and (3) are solved using Gummel's algorithm [10]. In order to analyze nonplanar devices such as CMOS structures, the finite-difference discretization is applied to these equations based on the box method [11], [12]. Applying the divergence theorem to the vector function $F = \nabla u$ at the cell S as shown in Fig. 1

$$\iint_S \nabla F\, dx\, dy = \int_l \nabla u \cdot \hat{n}\, dl. \tag{12}$$

The right-hand side is discretized at each cell. Then, except for boundaries, the discretization of Poisson's equation (1) becomes the five-point difference scheme, and the discretization of the current continuity equations (2) and (3) becomes the Scharfetter-Gummel difference scheme in two dimensions. The Scharfetter-Gummel difference scheme shows the upwind scheme for the convection terms of (2) and (3) and leads to stability in high field regions (cf. Appendix). In addition, the implicit-scheme is adopted for time-discretization of (2) and (3).

This simulation program uses the memory size of 2 M byte on the IBM3081K. In this work, typically about 7000 grid points are used for a 22×24 μm CMOS cross section, and CPU time is 2-3 h using one CPU of the IBM3081K.

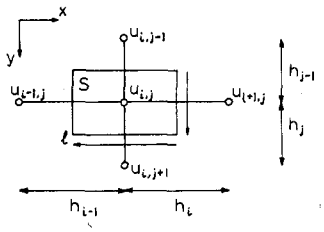

Fig. 1. Grid structure and cell for finite-difference discretization.

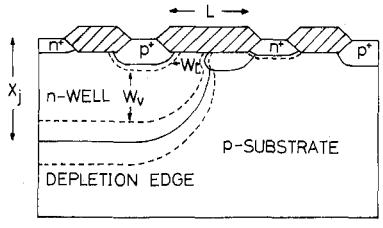

Fig. 2. n-well CMOS structure.

III. The Dynamics of Latchup Turn-On Behavior

A. CMOS Structure

A typical 2-D cross section of an n-well CMOS structure is shown in Fig. 2. Device parameters of the CMOS structure consist of the parts of vertical and lateral dimensions. The n-well junction depth x_j of the vertical dimensions is determined by the choice of a CMOS process. The n^+-p^+ spacing L of the lateral dimensions depends on the layout rules of CMOS integrated circuits. Therefore, even if one CMOS process is established, various kinds of CMOS structures are available in CMOS integrated circuits. In general, although the n-well junction depth x_j must be scaled down with reducing the minimum n^+-p^+ spacing, the pinched n-well resistance increases with the reduction of x_j in a standard bulk CMOS process. Therefore, it is difficult to scale down the vertical dimensions proportionally to the lateral dimensions because of the decrease in the latchup immunity of the CMOS circuits.

In this work, two types of CMOS structure with 6-μm n^+-p^+ spacing on the mask are investigated as shown in Fig. 3(a) and (b). Structure A is formed by applying a standard 2-μm n-well CMOS process [13] to the 6-μm n^+-p^+ spacing. This structure has a substrate doping of 1.0×10^{15} cm^{-3}, a 4.8-μm-deep n-well, and an n-well resistance of 2.3 k$\Omega/\square$. In this structure, the relation between the effective vertical and lateral base widths W_V, W_L of the parasitic p-n-p transistor is $W_L < W_V$, because scaling down in the n-well junction depth is neglected. As shown in Fig. 4, it is necessary for distance d from the p^+ to the n-well implantation edge to be longer than 1.7 μm on the mask in order to satisfy $W_L > W_V$. So, the n^+-p^+ spacing should be longer than 7.7 μm on the mask. Moreover, the parasitic PMOSFET turn-on voltage in structure A is measured as low as 6.3 V because of the phosphorus lateral diffusion of the n-well. This structure cannot be applied to actual integrated circuits without using both n- and p-channel stops similar to a p-well process. On the other hand, structure B has a scaled 3.0-μm-deep n-well by using a so-called retrograde

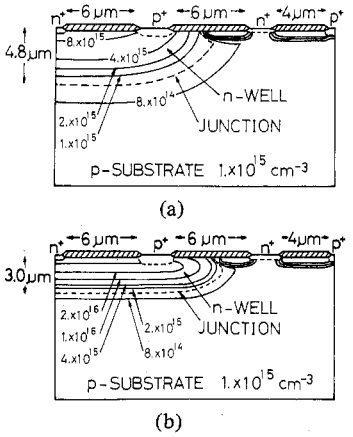

Fig. 3. Two-types of CMOS structure: (a) structure A and (b) structure B.

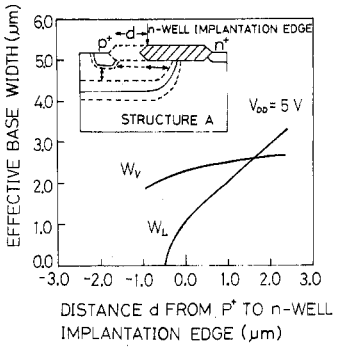

Fig. 4. Calculated effective lateral and vertical base widths of the parasitic p-n-p transistor for the structure A as a function of the distance d from the p^+ to the n-well implantation edge.

n-well structure [14], [15] to keep approximately the same sheet resistance 1.6 kΩ/□ as that of structure A and $W_V < W_L$.

B. Surface-Induced Latchup Triggering by the Parasitic PMOSFET

Transient current flow paths for typical surface-induced latchup can be examined by investigating latchup turn-on behavior triggered by the parasitic PMOSFET in structure A with the parasitic poly-Si gate. Fig. 5 shows measured latchup dc characteristics of fabricated structure A with the parasitic poly-Si gate over the field oxide when overvoltages are applied. Fig. 6 shows electrostatic potential of this structure at $t = 0$ when the parasitic poly-Si gate $V_G = 0$ V and the power supply voltage $V_{DD} = 7.9$ V are applied as step functions. In this work, electrostatic potentials are calculated as the Fermi level in intrinsic silicon at zero bias is zero potential. Fig. 7 shows electron and hole collector currents at the n-well/p-substrate junction as a function of time. As shown in the hole collector current, the parasitic PMOSFET turns on at $t = 110$ ps. The voltage drop caused by this hole current turns on the parasitic n-p-n transistor, which registers as electron current in the n-well. The electron current flowing into the n-well, however, does not lead to an increase of the hole current enough to increase the electron current from the n^+. Therefore, both electron and hole currents approach a steady-state value.

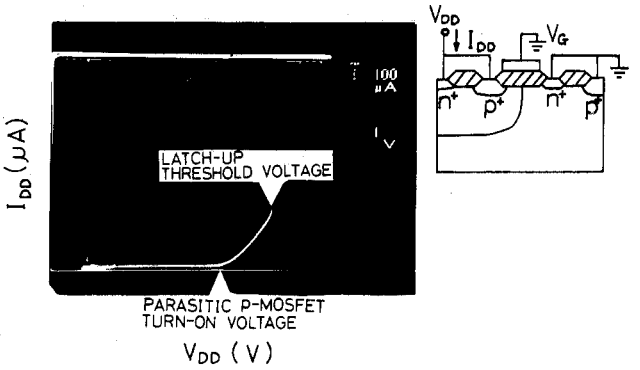

Fig. 5. Measured latchup dc characteristics of the fabricated structure A with the parasitic poly-Si gate. Vertical and horizontal axes are the supply current (100 μA/div) and the power supply voltage (1 V/div), respectively.

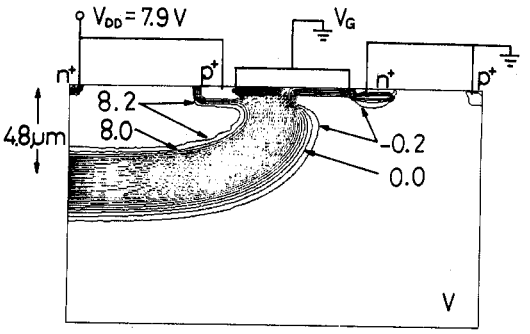

Fig. 6. Electrostatic potential of the structure A with the parasitic poly-Si gate at $t = 0$. The parasitic poly-Si gate voltage $V_G = 0$, and the power supply voltage $V_{DD} = 7.9$ V.

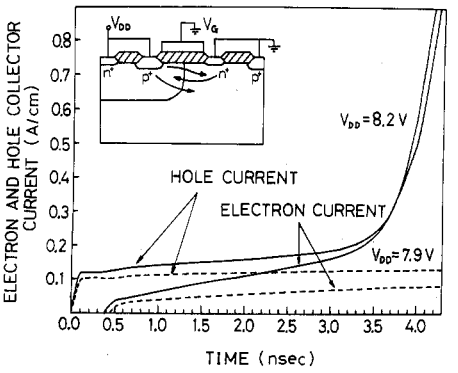

Fig. 7. Electron and hole collector currents at the n-well/p-substrate junction for structure A as a function of time. The dashed lines and the solid lines show the currents at $V_G = 0$ V and $V_{DD} = 7.9$ V, and $V_G = 0$ V and $V_{DD} = 8.2$ V, respectively.

On the other hand, when $V_G = 0$ V and $V_{DD} = 8.2$ V are applied as step functions, the electron collector current I_{cn} continues to increase with $(d^2I_{cn})/(dt^2) > 0$ from $t = 0.7$ ns. Fig. 8 shows lateral electric field for structure A. Electrons are accelerated toward the n-well by the lateral electric field $1.0\text{-}2.0 \times 10^3$ V/cm, which is set up by the hole current through the p-substrate, and flow into the n-well by the high electric field between the n-well and the p-substrate. Therefore, the lateral n-p-n transistor operates near the surface as indicated in Fig. 9(a). On the other hand, the parasitic p-n-p

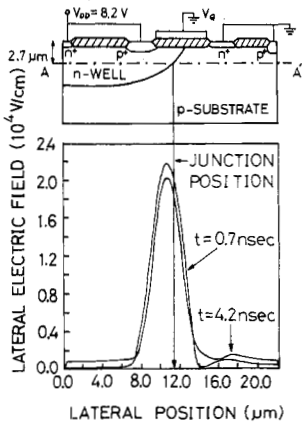

Fig. 8. Lateral electric fields at $t = 0.7$ ns and $t = 4.2$ ns for structure A. $V_{DD} = 8.2$ V. $V_G = 0$ V.

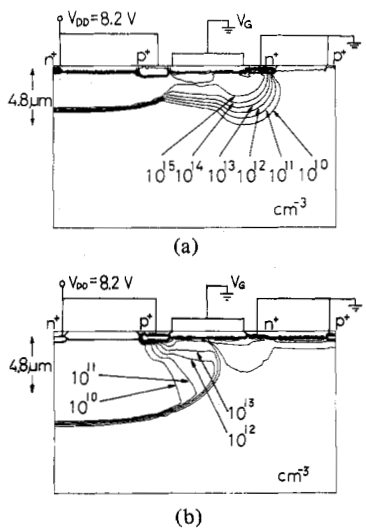

Fig. 9. Electron and hole densities at $t = 3.1$ ns. $V_{DD} = 8.2$ V. $V_G = 0$ V. (a) Electron density. (b) Hole density.

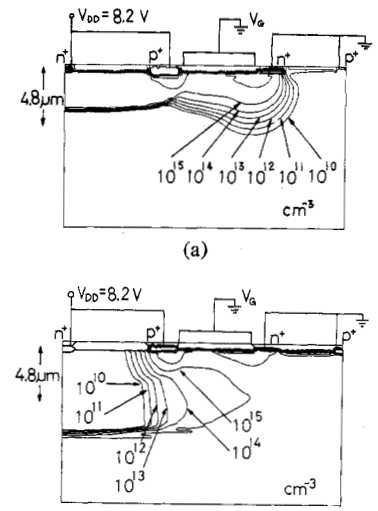

Fig. 10. Electron and hole densities at $t = 4.2$ ns for structure A. $V_{DD} = 8.2$ V. $V_G = 0$ V. (a) Electron density. (b) Hole density.

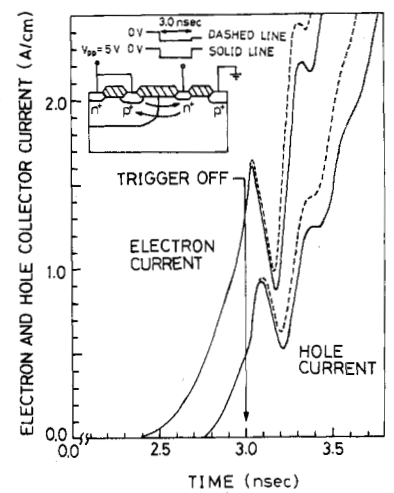

Fig. 11. Electron and hole collector currents at the well junction of structure A as a function of time. The dashed lines and the solid lines show the currents after a step voltage pulse is removed to 0 V and −0.57 V at 3.0 ns, respectively.

transistor operates in a lateral mode at $t = 3.1$ ns as indicated in Fig. 9(b). This is because the n-well surface underneath the field oxide is depleted and inverted which reduces the emitter-base potential barrier of the p-n-p transistor near the surface and consequently favors the hole injection near the surface. The regeneration action of the positive feedback starts and causes the rapid increase of both electron and hole currents as shown in Fig. 7. During the regeneration loop, as shown in Fig. 10(a), the electron current path is within the n-well junction depth. The hole current path is in a lateral mode due to $W_L < W_V$ in structure A rather than due to the influence of the parasitic poly-Si gate as shown in Fig. 10(b). Since both p-n-p and n-p-n transistors are operating in a lateral mode, the p-n-p-n operates in a lateral mode near the surface.

C. Surface-Induced Latchup Triggering by Direct Forward Biasing

Fig. 11 shows the electron and hole collector currents at the n-well junction of structure A as a function of time when a step voltage pulse is applied to the n^+ from $t = 0$ to 3.0 ns. The forward bias voltage is −0.76 V. The solid lines and the dashed lines show the electron and hole collector currents after the pulse is removed to 0 V and −0.57 V at $t = 3.0$ ns, respectively.

Before the stimulus is removed, the parasitic n-p-n transistor begins to be active at $t = 2.4$ ns, and the electron collector current increases rapidly. On the other hand, the parasitic p-n-p transistor begins to be active at $t = 2.8$ ns. Since the lateral electric field in the p-substrate is not generated and the effective base width of the p-n-p transistor is in the lateral direction, this time $t = 2.8$ ns is approximately estimated as the sum of both base transit times $W_{Bn}^2/2D_n + W_{Bp}^2/2D_p$, where W_{Bn} and W_{Bp} are the effective base widths of parasitic bipolar transistors. Actually, as shown in the electrostatic potential and the electron density at $t = 2.9$ ns in Fig. 12(a) and (b), there is no electrostatic potential modulation by the hole current flowing into the p-substrate, which is different from the case of triggering by the parasitic PMOSFET, and electrons deeply diffuse

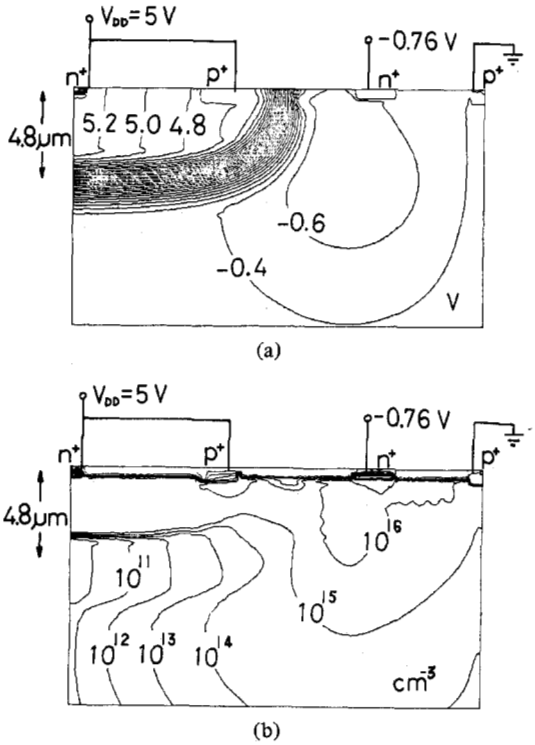

Fig. 12. Electrostatic potential and the electron density at t = 2.9 ns for structure A: (a) electrostatic potential and (b) electron density.

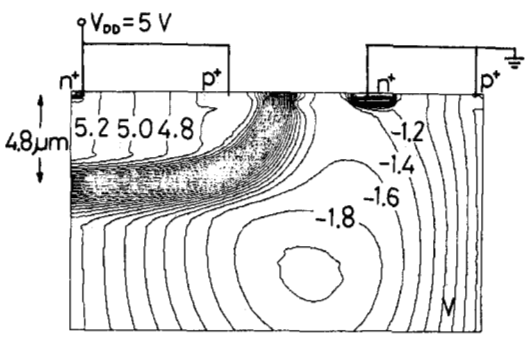

Fig. 13. Electrostatic potential at t = 3.06 ns for structure A after the stimulus is removed.

into the p-substrate. The current path in the latched state is always in the surface mode for structure A.

After the stimulus is removed as a step function at t = 3.0 ns, the regeneration loop can be observed from t = 3.18 ns. This regeneration loop time is estimated as 200 ps by the interval of locally minimum points of the electron collector current or the hole collector current. In fact, from t = 3.0 ns to t = 3.18 ns, the base area electrostatic potential of the parasitic n-p-n transistor is modulated in reverse-biased mode by electrons as indicated in Fig. 13. The electron collector current, however, reincreases from t = 3.18 ns by the hole collector current which is increasing until t = 3.08 ns. Therefore, the reincrease of the electron current in the case of the incomplete stimulus recovery (the dashed line) occurs at higher current level than that in the case of the complete stimulus recovery (the solid line). Fig. 14(a), (b), and (c) shows the electrostatic potential, the electron current density, and the hole current density at

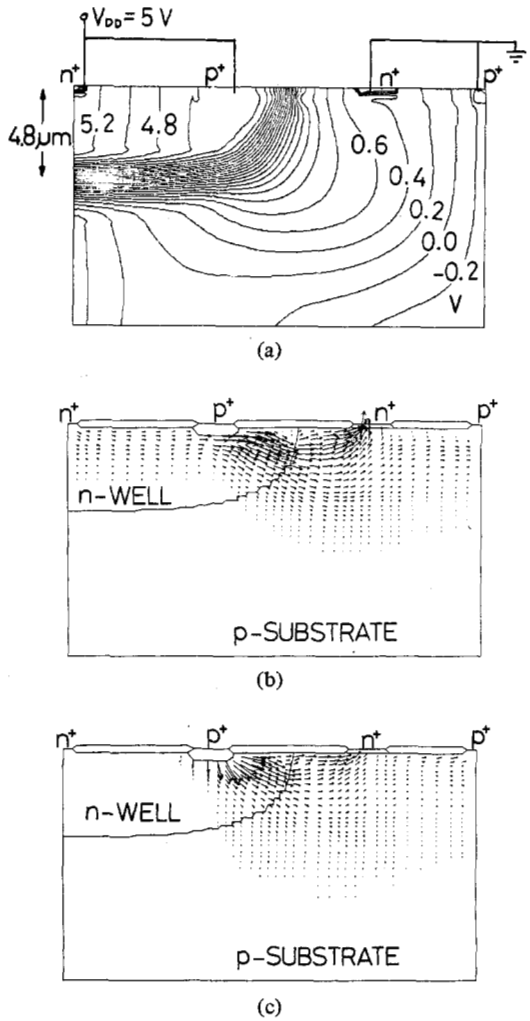

Fig. 14. Electrostatic potential, electron current density, and hole current density at t = 3.4 ns for structure A after latchup turn-on. (a) Electrostatic potential. (b) Electron current density. (c) Hole current density.

t = 3.4 ns during regeneration loop, respectively. The p-substrate electrostatic potential shows that the hole current injected from the p^+ flows toward the lateral direction. At the beginning of latchup turn-on, the parasitic p-n-p-n path also operates in a lateral mode near the surface as shown in electron and hole current densities in Fig. 14(b) and (c). With the increase of the hole and electron currents, the CMOS structure enters a low impedance state.

IV. Discussion

As shown in the two types of latchup turn-on behavior for structure A in Section III, the p-substrate potential is modulated to reverse- and forward-bias states by electrons or holes flowing through the p-substrate. Therefore, the electrostatic potential modulation in the p-substrate will be influenced as functions of the time and the current flow paths during latchup turn-on. Since, however, the parasitic n-p-n transistor action is essentially lateral in both cases of the electron current independent of drift or diffusion transport mechanisms, the n-well structure determines whether the parasitic p-n-p-n path is in the surface mode or not at the beginning of latchup

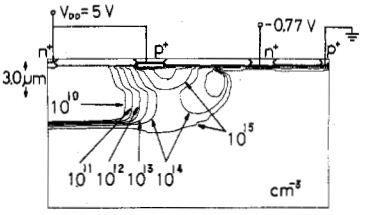

Fig. 15. Hole density at $t = 2.9$ ns for structure B. The n^+ is forward biased at −0.77 V.

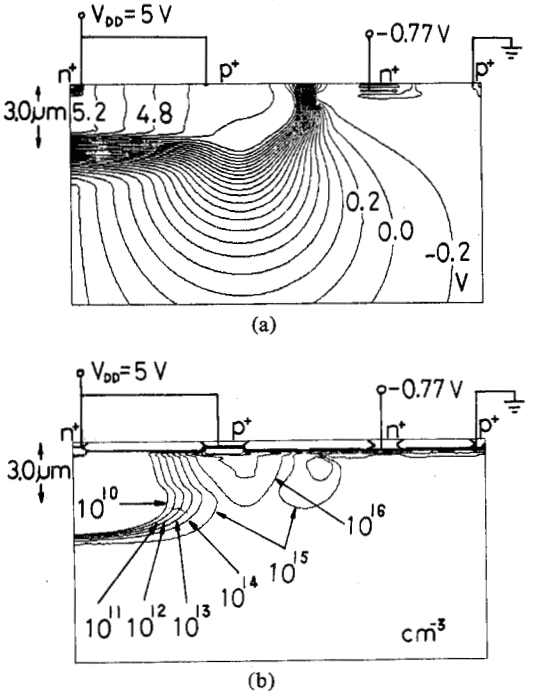

Fig. 16. Electrostatic potential and hole density at $t = 3.4$ ns for structure B with the stimulus on: (a) electrostatic potential and (b) hole density.

turn-on. Even in the case of structure B with $W_V < W_L$, as shown in Fig. 15, the parasitic p-n-p transistor starts in vertical action at the beginning of the turn-on, then the effective base area is pushed out toward the vertical direction with the increase of the hole current, and finally the hole current begins to flow toward the lateral direction as shown in Fig. 16(a) and (b). Therefore, in reducing the lateral dimensions in CMOS structures, the ratio of the effective lateral and vertical base widths will become an important factor for improving optimum latchup immunity of scaled CMOS structures. Moreover, the two-dimensional action of the parasitic p-n-p transistor depending on this factor decreases the effects of a low-resistive substrate. In particular, applying a low-resistive substrate to a CMOS process, the epi-layer thickness is an important device parameter for achieving high latchup immunity of scaled epi-CMOS. As shown in Fig. 17, this factor controlling the hole current flow paths will also play an important role for the determination of the epi-layer thickness.

V. Summary

The dynamics of latchup turn-on behavior in scaled CMOS structures have been examined using exact time-dependent and two-dimensional analysis based on the finite-difference approach. Both the dynamics of surface-induced latchup triggering by the parasitic PMOSFET and direct forward biasing have been compared to investigate the two-dimensional effects of parasitic devices during latchup turn-on. Although the electrostatic potential is modulated to the reverse- or forward-bias states by the carrier density, the n-well structure essentially determines whether the parasitic p-n-p-n path is in the surface mode or not at the beginning of latchup turn-on. Therefore, the ratio of the lateral and vertical effective base widths plays an important role for improving scaled CMOS latchup immunity.

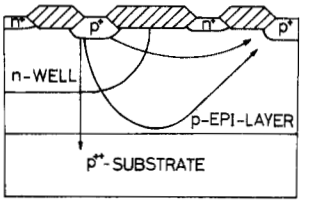

Fig. 17. Schematic hole current flow paths.

Appendix

In this Appendix, the Scharfetter-Gummel discretization is discussed. The Scharfetter-Gummel finite-difference scheme is shown to become the upwind scheme for the convection terms of the continuity equations at high electric field regions. The upwind scheme is often used to discretize the diffusion equation with the convection term for stability.

After the normalization, the electron current density equation is described in the following form:

$$J_n = \mu_n \nabla n - \mu_n n \nabla \psi. \tag{A1}$$

In the right-hand side, the first term shows the diffusion term, and the second term is regarded as the convection term. If it is assumed that the generation-recombination term and the avalanche generation term are neglected, the electron continuity equation becomes

$$\nabla J_n = 0 \tag{A2}$$

in the steady state. Equation (A2) can be rewritten as the following form:

$$\frac{\partial}{\partial x}\mu_n e^{\psi}\frac{\partial}{\partial x}(e^{-\psi}\cdot n) + \frac{\partial}{\partial y}\mu_n e^{\psi}\frac{\partial}{\partial y}(e^{-\psi}\cdot n) = 0. \tag{A3}$$

The Scharfetter-Gummel discretization of the continuity equation (A3) is based on the following evaluation of e^{ψ} at a interval $[x_{i,j}, x_{i+1,j}]$

$$(e^{\psi})_{i+1/2,j} = \begin{cases} \dfrac{\psi_{i+1,j} - \psi_{i,j}}{e^{-\psi_{i,j}} - e^{-\psi_{i+1,j}}}, & \psi_{i+1,j} \neq \psi_{i,j} \\ e^{\psi_{i,j}}, & \psi_{i+1,j} = \psi_{i,j}. \end{cases} \tag{A4}$$

Using this evaluation, the x electron current component J_x (the y component J_y is obtained similarly) can be discretized

$$J_{x_{i+1/2,j}} = -\mu_{n_{i+1/2,j}} \frac{\psi_{i+1,j} - \psi_{i,j}}{h_i} \left(\frac{n_{i+1,j}}{1 - e^{\psi_{i+1,j} - \psi_{i,j}}} + \frac{n_i}{1 - e^{\psi_{i,j} - \psi_{i+1,j}}} \right). \quad (A5)$$

Let $\psi_{i+1,j} - \psi_{i,j} >> 1$ and $\eta = e^{\psi_{i,j} - \psi_{i+1,j}}$, then

$$\frac{1}{1 - e^{\psi_{i+1,j} - \psi_{i,j}}} = -e^{\psi_{i,j} - \psi_{i+1,j}} [1 + e^{\psi_{i,j} - \psi_{i+1,j}} + 0(\eta^2)] \quad (A6)$$

and

$$\frac{1}{1 - e^{\psi_{i,j} - \psi_{i+1,j}}} = 1 + e^{\psi_{i,j} - \psi_{i+1,j}} + 0(\eta^2). \quad (A7)$$

Using (A6) and (A7) to (A5)

$$J_{x_{i+1/2,j}} = \mu_{n_{i+1/2,j}} (\psi_{i+1,j} - \psi_{i,j}) [e^{\psi_{i,j} - \psi_{i+1,j}} + 0(\eta^2)] \cdot \frac{n_{i+1,j} - n_{i,j}}{h_i} - \mu_{n_{i+1/2,j}} n_{i,j} \frac{\psi_{i+1,j} - \psi_{i,j}}{h_i}. \quad (A8)$$

Similarly, if $\psi_{i,j} - \psi_{i+1,j} >> 1$ and $\eta = e^{\psi_{i+1,j} - \psi_{i,j}}$, then

$$J_{x_{i+1/2,j}} = \mu_{n_{i+1/2,j}} (\psi_{i,j} - \psi_{i+1,j}) [e^{\psi_{i+1,j} - \psi_{i,j}} + 0(\eta^2)] \cdot \frac{n_{i+1,j} - n_{i,j}}{h_i} - \mu_{n_{i+1/2,j}} n_{i+1,j} \frac{\psi_{i+1,j} - \psi_{i,j}}{h_i}. \quad (A9)$$

Therefore, in the form $v = \mu_n E$, the difference scheme of the convection term

$$(\nabla v \cdot n)_{x_{i,j}} = \begin{cases} \frac{2}{h_i + h_{i-1}} (\mu_{n_{i+1/2,j}} E_{i+1/2,j} n_{i,j} - \mu_{n_{i+1/2,j}} E_{i-1/2,j} n_{i-1,j}), & E_{i+1/2,j} < 0 \\ \frac{2}{h_i + h_{i-1}} (\mu_{n_{i+1/2,j}} E_{i+1/2,j} n_{i+1,j} - \mu_{n_{i+1/2,j}} E_{i-1/2,j} n_{i,j}), & E_{i+1/2,j} > 0 \end{cases} \quad (A10)$$

shows the upwind scheme, where $E = -\nabla\psi$. The same result is obtained for the hole current.

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