Double Pocket Architecture Using Indium and Boron for Sub-100 nm MOSFETs

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***Abstract*—A double pocket architecture for sub-100 nm MOSFET's is proposed on the basis of indium pocket profiling at higher dose than the amorphization threshold. At high dose, the low-energy indium pockets realize the improvement of short channel effects and shallow extension formation of highly doped drain, maintaining the low junction leakage level. Double pocket architecture using indium and boron is demonstrated in a 70 nm gate length MOSFET with high drive currents and good control of the short channel effects.**

***Index Terms*—Indium diffusion, junction leakage current, MOSFET, pocket profile.**

I. Introduction

THE scaling down of MOSFETs is accelerated into the sub-100 nm regime to meet the continuing trend of low power consumption and high-speed device performance. The pocket profiles in scaled devices have an impact on formation of shallow source–drain extensions and nonuniform channel profiles and hence the pocket profiling, which is strongly correlated to the diffusion mechanism of dopants, is a key issue to achieving high device performance.

Indium was recommended for fabricating steep retrograde channel profiles due to the heavy ion atom and the strong segregation to oxide [1]–[3], and shallow source–drain extensions with pre-amorphization for the dechanneling [4], [5]. For indium pocket profiling, two approaches, that is, low-dose tilted ion implantation [6] and high-dose ion implantation [7], have been explored.

This paper describes double pocket architecture using indium and boron for a sub-100 nm MOSFET structure on the basis of indium pocket profiling at higher dose than the amorphization threshold ($\sim 5 \times 10^{13}\text{cm}^{-2}$) [8], [9]. At high dose, the low-energy indium pockets realize the improvement of short channel effects and shallow extension formation of highly doped drain, maintaining the low junction leakage level. Double pocket architecture using indium and boron is demonstrated in the sub-100 nm regime with high drive currents and good control of the short channel effects.

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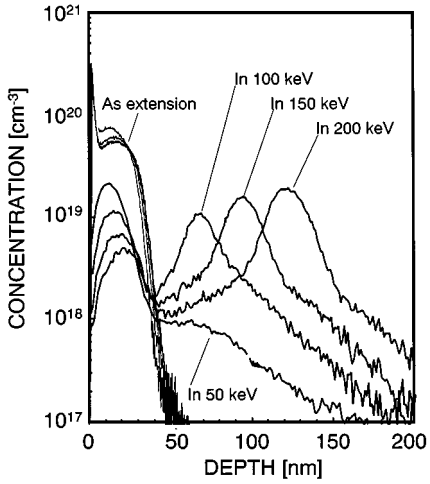

Fig. 1. SIMS profiles of indium pockets and arsenic source–drain extensions for different indium energies of 50 keV, 100 keV, 150 keV, and 200 keV. Indium is implanted at tilted angle of 7° for a high dose of 1×10^{14} cm^{-2}. All dopants are activated by a two-step RTA annealing at 950 °C for 10 s after extension and pocket implantation, and at 1000 °C for 10 s after deep source–drain implantation.

II. Low-Energy, High Dose Indium Pocket Profiling

Recent diffusion studies of indium indicate that indium diffusion strongly depends on the implant damage and the damage profile after the indium implant [8], [9]. SIMS analysis of the shallow arsenic extensions and indium pocket profiles is shown in Fig. 1, indicating the energy dependence of indium implants at a high dose on the pocket profile. Indium was implanted into silicon at tilted angle of 7° for a high dose of 1×10^{14} cm^{-2} in the range of the implant energy from 50 keV to 200 keV. Source–drain extensions are formed by 8 keV arsenic implants with a dose of 5×10^{14} cm^{-2}. All dopants are activated by a two-step RTA annealing at 950 °C for 10 sec after extension and pocket implantation, and at 1000 °C for 10 s after deep source–drain implantation. The deep source–drain junction exists around 100 nm and the shallow extension depth is estimated to be 40 nm.

The indium pocket profiles for higher energy than 100 keV have two peaks of indium profiles as shown in our previous work [7]. The deeper peaks of indium are deeper than the as-implanted projected range. In fact, the as-implanted projected ranges are estimated to be 30.5 nm, 48.5 nm, 70.3 nm, and 82.9 nm, for 50 keV, 100 keV, 150 keV, and 200 keV, respectively [10]. It is confirmed by TEM images that the locus of deeper indium peaks corresponds to the initial amorphous/crystal interface at the depth of around 70 nm, 100 nm, 125 nm, respectively. The end-of-range dislocation loops during the

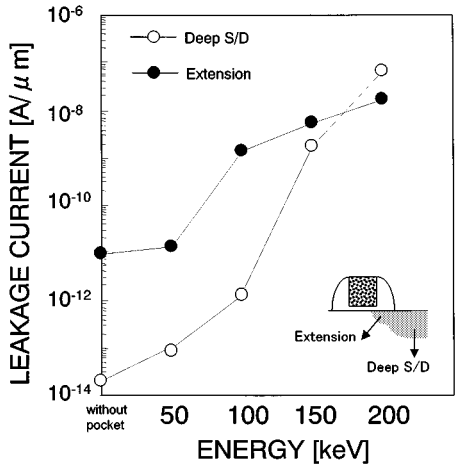

Fig. 2. Junction leakage current versus indium pocket implant energy for the devices shown in Fig. 1.

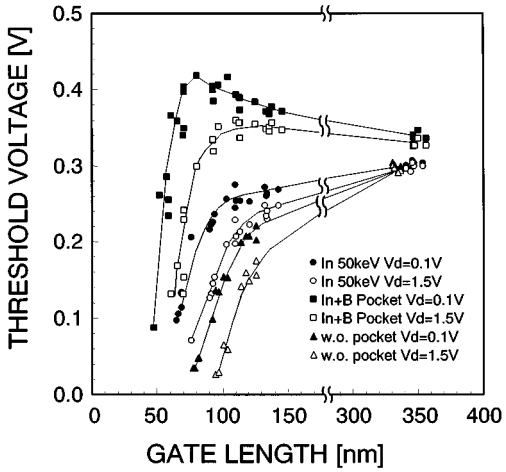

Fig. 3. Linear and saturated threshold voltage roll-off characteristics for three types of devices with single 50 keV, 8×10^{13} cm^{-2} indium pockets and without pockets, and with 20 keV, 8×10^{13} cm^{-2} indium and 10 keV, 3×10^{13} cm^{-2} boron double pockets, respectively.

annealing are generated below the amorphous/crystal interface and become the trap site of interstitials and dopants [8]. The 50 keV indium implants had little impact on the formation of EOR dislocation loops. The amorphous layer is re-crystallized by the annealing. As shown in Fig. 1, high dose indium implants at 50 keV exhibit a significant difference of diffusion behavior, indicating the different pocket profile formation. The indium segregates into the damage layer within the arsenic extensions, resulting in one peak profile of indium.

The junction leakage current characteristics were evaluated by using a test structure having a large junction area of 150×150 μm^2 and a MOS structure with a long gate length of 1 μm. The reverse leakage current at the bottom of deep source–drain is estimated at 1.5 V bias by using the test structure having a large junction area. The value of leakage current at the shallow extensions including the edge of deep source–drain is extracted from the off-state leakage of MOSFET at 1.5 V bias by estimating the reverse leakage current at the bottom of deep source–drain in the MOSFET structure.

Fig. 2 shows the junction leakage current versus indium implant energy characteristics for the devices shown in Fig. 1. The leakage current at the bottom of deep source–drain significantly decreases with the decrease of indium implantation energy. Since the deep source–drain junction depth is around 100 nm, this is consistent with the results of indium depth. For 50 keV energy case, the increase of junction leakage currents at the shallow extension is further suppressed, indicating the almost same leakage current level as that of the device without pockets.

III. Double Pocket Architecture using Indium and Boron

The low-energy, high dose indium pocket profiling allows the shallow junction formation of highly doped drain extensions and indium/boron double pocket architecture in the sub-100 nm regime. The sub-100 nm MOSFETs were fabricated with steep retrograde indium channel, highly doped source–drain extensions and indium/boron double pocket profiles. The physical gate oxide thickness is 1.8 nm. For the channel profile, indium is implanted at 100 keV for a dose of 1×10^{13} cm^{-2}. After gate electrode formation, 20 keV indium and 10 keV boron are implanted at tilted angle of 7° for total doses of 8×10^{13} cm^{-2} and 3×10^{13} cm^{-2}, respectively. Highly doped drain extensions are further formed by 2 keV arsenic implants with a high dose of 8×10^{14} cm^{-2}. Also, 50 keV, 8×10^{13} cm^{-2} indium implants are performed for a single indium pocket device. All dopants were activated by a two-step RTA annealing at 950 °C for 10 s after extension and pocket implantation, and at 1000 °C for 10 s after deep source–drain implantation. The leakage current at the extensions for a single indium pocket device was 1.54×10^{-11} A/μm, which is the almost same level as that shown in Fig. 2.

Fig. 3 shows the linear and saturated threshold voltage roll-off characteristics for three types of devices. It is found that no reverse short channel effect occurs for the indium channel devices with single indium pockets and without pockets even in linear threshold voltage due to the deactivation at the edge of extensions [11]. However, the indium channel device without pockets degrades the short channel effect, in particular, when using highly doped drain extensions. The single indium pocket device improves the short channel effect by 20 nm in minimum gate length. This implies that the low-energy, high dose indium pocket is effective in forming the shallow extensions of highly doped drain in the sub-100 nm regime. Moreover, the saturated threshold voltage can be adjusted by an assisted boron pocket, eliminating the reverse short channel effect at 1.5 V drain bias, while the device exhibits the reverse short channel effect in the linear threshold voltage at 0.1 V drain bias. Such a device architecture significantly improves the gate drive, which results in high saturated drive current.

The I_{on} versus I_{off} characteristics for three types of devices at 1.5 V drain bias is shown in Fig. 4. At 2.5 nA/μm off-current, nominal I_{on} of the single indium pocket device is increased from 740 μA/um to 820 μA/μm. The double pocket device further improves the short-channel effect and hence the device achieves the higher drive current of 885 μA/μm at an off-current of 2.5 nA/μm for a 70 nm gate length MOSFET.

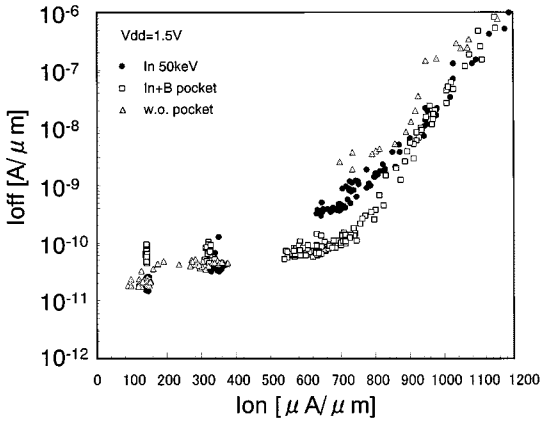

Fig. 4. I_{on} versus I_{off} characteristics for three types of devices at 1.5 V drain bias shown in Fig. 3.

IV. Conclusions

An indium/boron double pocket architecture has been proposed on the basis of indium pocket profiling at higher dose than the amorphization threshold. At high dose, the low energy indium pockets realize the improvement of short channel effects and shallow extension formation of highly doped drain, maintaining the low junction leakage level. This approach allows the double pocket architecture using indium and boron, which results in the high drive current and high immunity of short channel effect in the 70 nm gate length.

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