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A Design Hierarchy of IC Interconnects and Gate Patterns

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SUMMARY A new design hierarchy in TCAD is discussed with emphasis on a design of IC interconnects and gate patterns. Two design methodologies for gate patterns at a CMOS cell level and multilevel interconnect scheme at a chip level are proposed. This approach generates the layout design rules of gate patterns, considering the fabrication process and pattern layout dependency, and allows a design of multilevel interconnect scheme at the initial phase of technology development.

key words: *TCAD, interconnect, OPC, gate pattern, design rule*

1. Introduction

Technology Computer-Aided Design (TCAD) has played an important role in technology selection, design of fabrication processes and scaled silicon devices, process control, and a better understanding of physical phenomena inside the devices [1]. The scaled CMOS devices allow the development of high packing density, high speed, and low power LSIs. Miniaturization of CMOS devices now pushes against the physical limits of fabrication processes and devices and hence technology dependence of circuit design rapidly increases. In the deep-submicron regime, we have to touch the non-scalability of interconnect delays and lithography improvement to overcome unmanageable complexity between the manufacturing process development and circuit design.

The purpose of this paper is to describe a design hierarchy of IC interconnects and gate patterns. Design methodologies for gate patterns at a CMOS cell level and multilevel interconnect scheme at a chip level are proposed, which are applied at the initial phase of technology development. A design hierarchy of IC interconnects and gate patterns is discussed. Section 2 describes a new design hierarchy in TCAD. Section 3 discusses the layout design rule of gate patterns using an optical proximity correction (OPC). In Sect. 4, a chip level interconnect model is discussed to investigate multilevel interconnect scheme and a hierarchy of interconnect level.

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2. New Design Hierarchy in TCAD

In the development of LSIs, the fabrication process and LSI design have been coupled with a design rule. Design rules are a set of regulations which define the physical dimensions and electrical characteristics available for a new fabrication process. In the late 1970s, Mead and Conway proposed normalizing all of the layout dimensions in the design rules in terms of a scale factor, λ [2]. This unit, λ, involves etching variants and photoresist pattern tolerances as well as the mask alignment tolerance. If the layout design rules are changed, then only λ is changed. This approach allows a hierarchical design of LSIs, which is clearly separated from the fabrication process. The circuit designers can create circuit configurations to implement desired functions, circuits and systems independent of the complicated fabrication process. Unfortunately, the chip performance and manufacturability of real LSIs strongly depend on specific fabrication processes and hence we meet complexity between the new process development and circuit design.

Figure 1 shows a new design hierarchy in TCAD at the initial phase of technology development. The process and device models are primarily applied for an initial design of new fabrication processes and devices, coupling with the process development. An initial design of interconnects and gate patterns, however, requires not only process dependency but also targets of chip performance and information from cell layout design prior to starting the physical design of LSIs. This creates the need for a new design hierarchy of IC interconnects and gate patterns at the initial phase of technology development. We have to touch the non-scalability of the interconnect delays and lithography improvement to construct the new design hierarchy in TCAD.

3. Gate Pattern

Optical lithography continues to be the mainstream technology. Despite of wavelength resolution using advanced exposure tool, a resolution enhancement technique such as phase shift mask and optical proximity correction are further needed. The gate level lithography requires higher resolution than the general lithography and hence the optical proximity effect has a signifi-

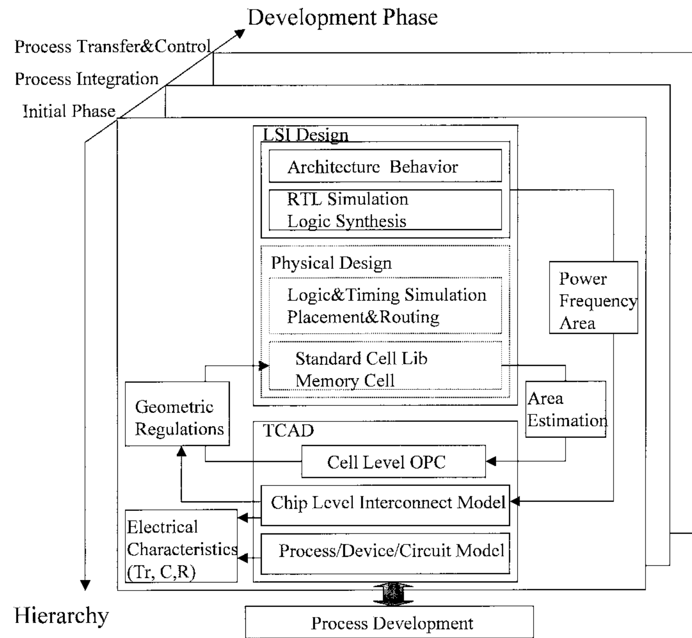


Fig. 1 Design hierarchy in TCAD at the initial phase of development.

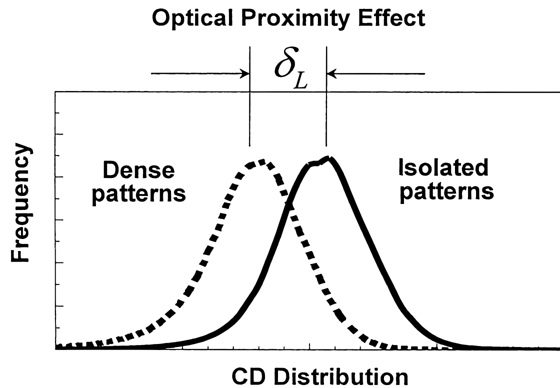


Fig. 2 Spreads of gate CD distributions for dense and isolated patterns.

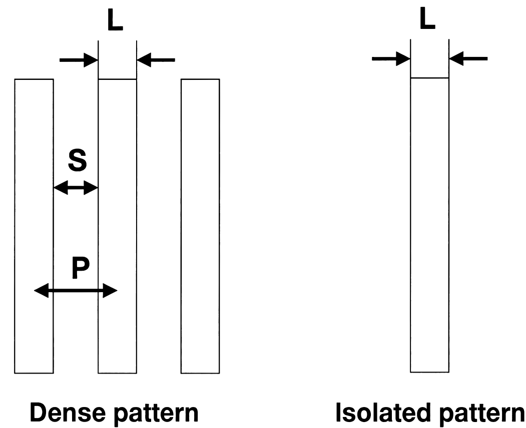


Fig. 3 Schematic view of dense and isolated patterns.

cant impact on the layout design rules of gate patterns.

Figure 2 shows spreads of gate CD distributions for dense and isolated patterns. The gate CD distributions are derived from the response surface function (RSF) for line and gap patterns by inputting an error distribution of process variables [3]. A schematic view of dense and isolated patterns is shown in Fig. 3. The difference δ_L between the printed dense and isolated patterns represents the optical proximity effect. Since there are some sorts of line and gap patterns in CMOS standard cells, this effect induces the difference between mask and printed pattern sizes at the cell level:

$$\Delta CD = |Lmask - L_p|. \qquad (1)$$

This means that circuit designers have to correct the layout design rule of gate patterns, considering both lithographic process and pattern layout dependency. Moreover, the difference ΔCD increases due to the optical proximity effect as the device dimension is scaled down. Figure 4 shows the ratio of $\Delta CD/$gate length at different gate pattern pitches. A significant increase of ΔCD in the $0.13\,\mu$m generation is recognized. In fact, $\Delta CD/$gate length reaches 40% using ArF lithography for the $0.13\,\mu$m generation while KrF capability for $0.18\,\mu$m generation exhibits $\Delta CD/$gate length of 7%.

The line-end shortening effect has another impact on the layout design of gate patterns. The gate pattern at the line end is shorten by

$$\delta = |lmask - l_p|. \qquad (2)$$

It is known that this difference is suppressed by cor-

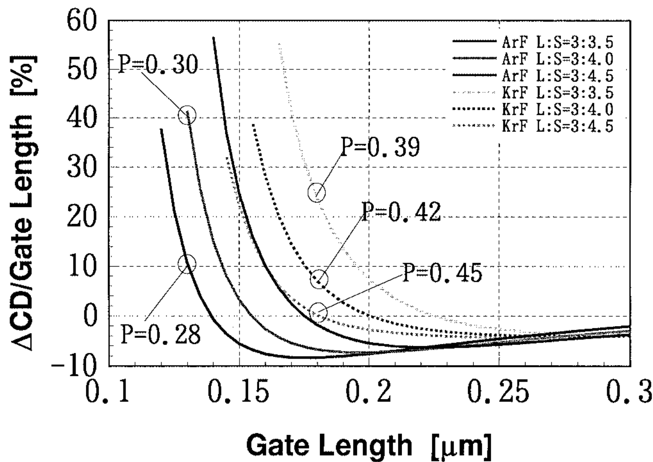


Fig. 4 ΔCD/gate length as a function of gate length at different gate pattern pitches.

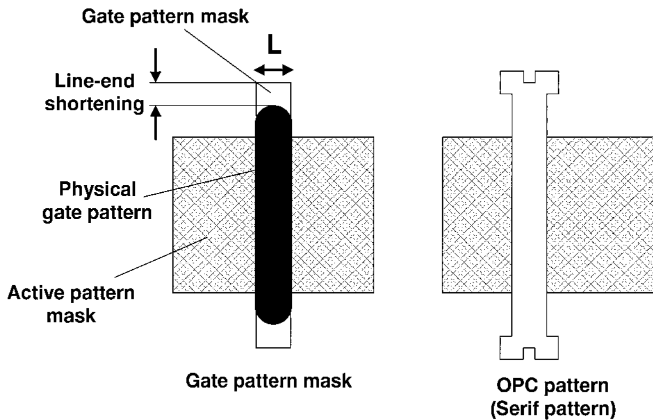


Fig. 5 Schematic view of the uncorrected and corrected line-end pattern.

rected patterns with serif patterns. A schematic view of uncorrected line-end patterns and corrected patterns with the serif patterns is shown in Fig. 5. Figure 6 shows the line-end shortening effect on uncorrected and corrected patterns when using ArF and KrF lithography, respectively. The simulations are performed using a 3D aerial image simulator. It is found that the line-end shortening effect is significantly enhanced with the reduction of gate length. The corrected patterns improve the line-end shortening, indicating that the layout design rule of gate patterns is decided by the corrected patterns. This creates the need for new design methodology for generating geometric regulations of gate patterns.

Figure 7 shows a flow chart of the calculation procedure for the layout design rules of gate patterns. The procedure includes a cell level OPC [4]. An initial design rule is given on the basis of resolution capability of optical lithography at each generation. Original mask patterns at a CMOS standard cell level are designed.

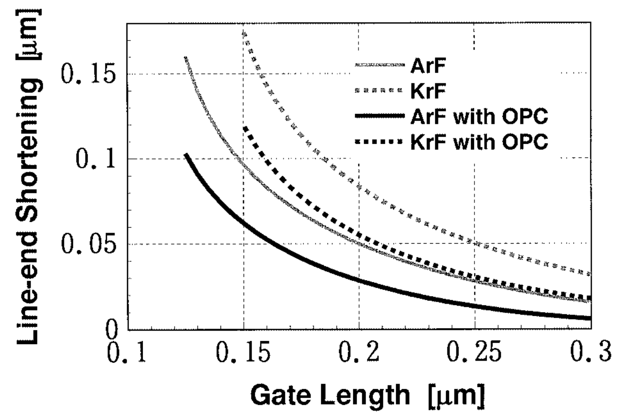


Fig. 6 The line-end shortening effect on uncorrected and corrected gate patterns when using ArF and KrF lithography.

After the gate figures are extracted from a CMOS cell layout patterns, OPC mask patterns are generated using serif patterns and intersection patterns. Then, the printed patterns are simulated by using a 3D aerial image simulator. The 3D simulator allows the calculation as a function of process variables such as exposure dose and focus position and hence OPC mask patterns can be designed considering process latitude. The result is checked comparing with the original mask patterns. If the difference of mask and printed patterns is too large, the layout design rules are modified. After an iterative procedure, the approach provides the mask patterns in CMOS cells, considering the fabrication process and pattern layout dependency, and allows the cell size reduction at the initial phase of process development.

4. Interconnect

The interconnect RC delay significantly impacts the chip performance in the deep-submicron regime. A hierarchy of interconnect levels is required because of the non-scalability of the interconnect delays [5]. At each technology generation new interconnect materials have to be selected at the initial phase of development. Unfortunately, for interconnect modeling a chip level model is required to investigate interconnect performance and design rules of interconnects, including both impact of process technology and circuit design techniques.

To calculate interconnect delays, a chip level delay model is developed as shown in Fig. 8 [6]. Interconnects of LSI chip are divided by mainly two parts, power line and signal line. The power line is modeled as a meshed network and uniformly distributed current sources. Delay time with wiring load for signal lines is calculated on the basis of Sakurai's formula [7],

$$\tau_{pd} = kR_W C_W + R_W C_g + R_g C_W + R_g C_g \qquad (3)$$

where k is a proportional coefficient, R_W is the wiring

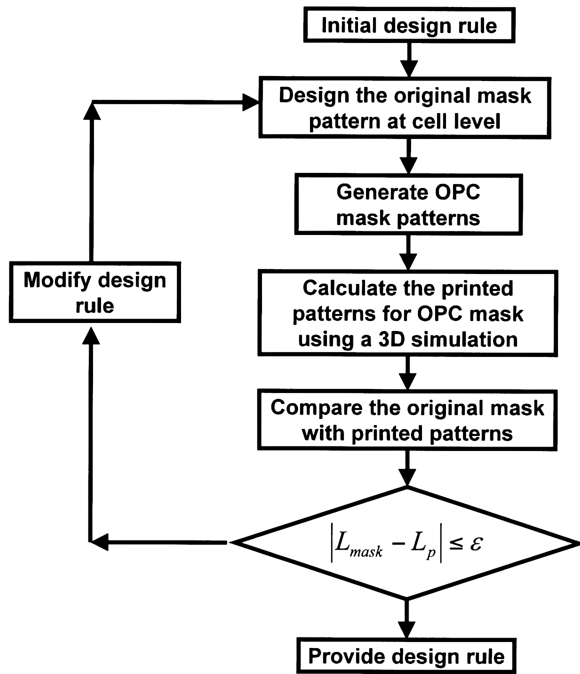


Fig. 7 Flow chart of the calculation procedure for the layout design rules of gate patterns.

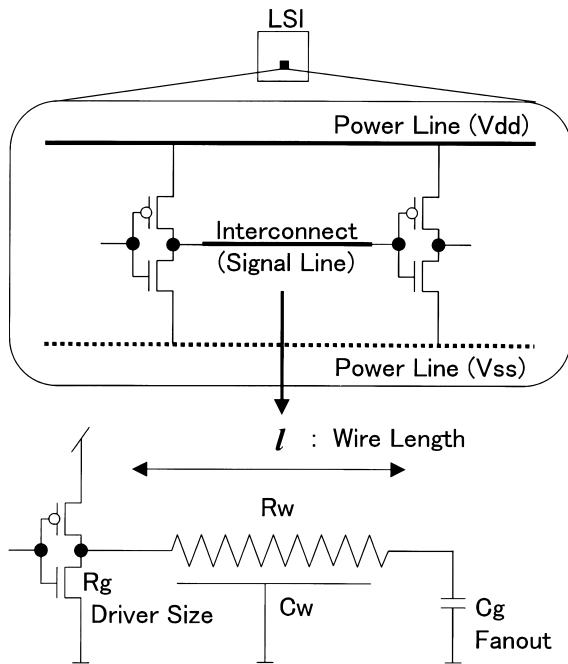


Fig. 8 Chip level delay model.

resistance, C_W is the wiring capacitance, R_g is the resistance of driver size, C_g is the transistor capacitance of fanout.

To develop the chip level delay model, the wiring resistance R_W and capacitance C_W are calculated using a stochastic wire-length distribution model at a chip level [8] and cross sectional structure of interconnect

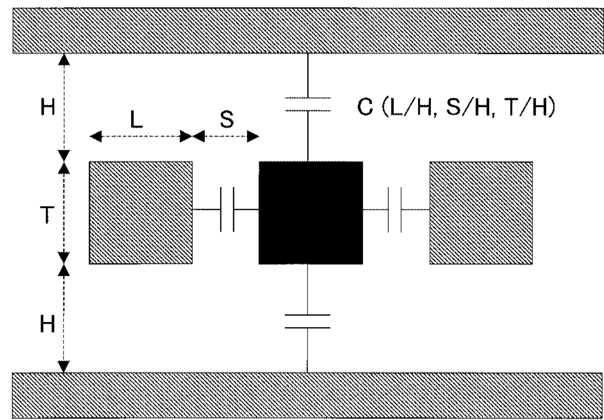


Fig. 9 Cross sectional structure of interconnect and metal and vertical pitches.

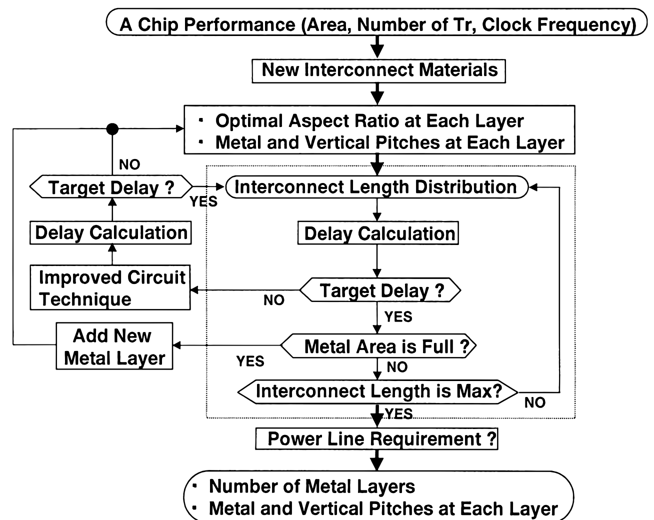


Fig. 10 Flow chart of design methodology for multilevel interconnect scheme.

[6].

$$C_W = C(L/H, S/H, T/H) \times l, \tag{4}$$

$$R_W = R(L, T) \times l, \tag{5}$$

where l is a wire-length distribution at a chip level. A two-dimensional cross sectional structure of interconnect and metal pitch is defined as the line width L, line space S, line thickness T and dielectric thickness as shown in Fig. 9. The total capacitance C, which is expressed by the summation of the lateral capacitance C_L and vertical capacitance C_V as a function of L/H, S/H, and T/H, is calculated by a table look-up model for two-dimensional capacitance. The calculation of wiring resistance R_W further includes the effect of barrier metal.

Figure 10 shows a flow chart of design methodology for multilevel interconnect scheme. This procedure

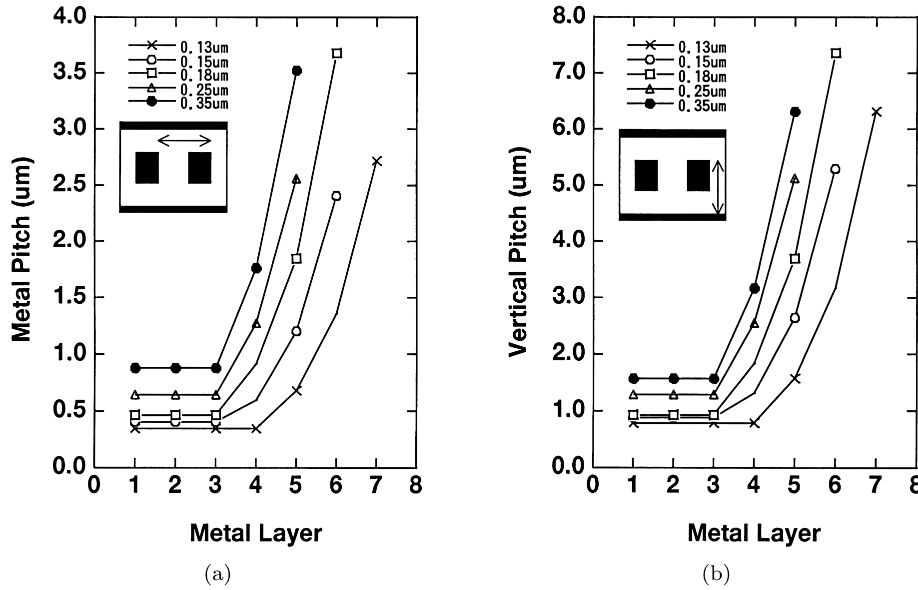


Fig. 11 The scaling of (a) metal pitch and (b) vertical pitch at each layer.

Table 1 LSI performance trend (SIA roadmap).

	Design Rule	um	0.35	0.25	0.18	0.15	0.13
Chip Performance	Number of Transistor	million	6	11	21	40	76
	Clock Frequency	MHz	300	400	600	700	800
	Chip Area	mm2	250	300	340	385	430
Device Technology Parameters	Power Supply	V	3.3	2.5	1.8	1.5	1.2
	Threshold Voltage	V	0.60	0.48	0.38	0.34	0.30
	Gate Oxide Thickness	nm	7.0	5.0	3.5	3.0	2.5
	Nch Drain Current	uA/um	600	600	600	600	600
	Pch Drain Current	uA/um	280	280	280	280	280
Interconnect Technology Parameters	Conductivity		3.3	3.3	2.2	2.2	2.2
	Permittivity		4.1	4.1	3.0	2.5	2.0
	Local Line Width	um	0.44	0.32	0.23	0.20	0.17
	Local Line Space	um	0.44	0.32	0.23	0.20	0.17
	Local Line Thickness	um	0.70	0.58	0.41	0.40	0.36
	Dielectric Thickness	um	0.88	0.70	0.51	0.48	0.43

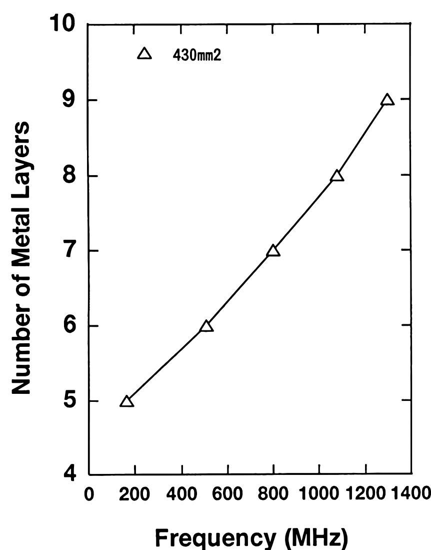
also accounts for change of driver size, insertion of repeaters and variable pitch router as improved circuit design techniques [5]. Optimal aspect ratio and metal pitch at each layer are calculated as a design rule at each technology generation. When the number of transistors, chip area, and clock frequency are given, the number of metal layers, metal pitch, and optimal aspect ratio are predicted as a design rule at each generation, indicating the impact of new interconnect materials and improved circuit techniques.

In general, the clock period is estimated by a critical path, which consists of a certain number of average stages loaded by average interconnects plus the one driving a global interconnect. In this work, target delay for semi-global and global interconnects is assumed to be 20% of the clock period. If the delay time does not reach target delay, the design rule of interconnect and interconnect materials are changed. The wiring area at each metal level is calculated by the product of metal pitch, total interconnect length, and wiring efficiency (= 0.4). If the metal area exceeds a chip size, a new metal layer is added. This methodology provides a means for predicting a design rule of interconnect at a chip level.

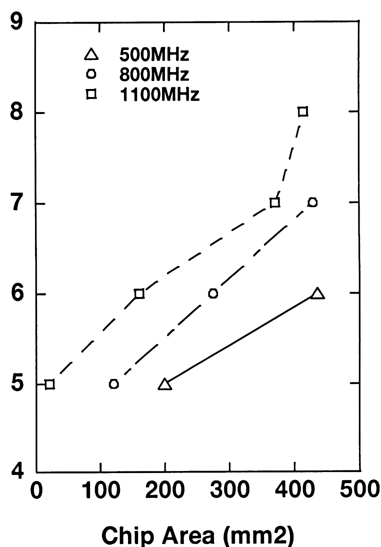
Figures 11(a) and (b) show the scaling of the metal pitch and vertical pitch at each layer for high performance LSIs. The initial interconnect parameters such as interconnect materials, aspect ratio, and metal pitch are derived from the 1997 version of SIA Roadmap [9]. Table 1 summarizes chip performance, device and interconnect technology parameters. Selection of new materials at each generation is plotted in Table 2. The metal

Table 2 Selection of new materials at each technology generation.

New Materials		
Generation	Material	k
0.13um	Cu	2.0
0.15um	Cu	2.5
0.18um	Cu	3.0
0.25um	Al	4.1
0.35um	Al	4.1



(a)



(b)

Fig. 12 The number of metal layer versus (a) clock frequency and (b) chip area, respectively.

pitch of local interconnect is scaled down by the factor of κ and the vertical pitch by the factor of $\sqrt{\kappa}$ at each generation. However, the design rule of global interconnect for a high performance LSI is almost constant from 0.35 μm to 0.13 μm generation. It is found that a LSI in the 0.13 μm generation needs 7 metal layers and a hierarchy of 4 interconnect levels.

Figures 12(a) and (b) show the number of metal layers for 0.13 μm LSIs as a function of clock frequency and chip area, respectively. The clock frequency and chip area are important targets of LSIs, which are determined from analysis of architecture behavior and RTL simulations. For a high performance LSI with higher clock frequency, the number of metal layer increases as shown in Fig. 12(a). In this case, target delay for semi-global and global interconnects is assumed to be 20% of the clock period. When the chip area becomes smaller, the number of metal layer for a LSI having chip area of 100 mm^2 decreases down to 5. Thus this methodology allows the development of multilevel interconnect schemes for a wide variety of LSIs.

5. Conclusion

A design hierarchy of IC interconnects and gate patterns has been discussed. Two design methodologies have been proposed for designing gate patterns at a CMOS standard cell level and multilevel interconnect scheme at a chip level. This approach generates the layout design rules of gate patterns, considering the fabrication process and pattern layout dependency, and allows a design of multilevel interconnect scheme at the initial phase of technology development.

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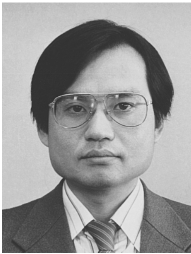

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