A NUMERICAL SIMULATION OF HOT-CARRIER INDUCED DEVICE DEGRADATION

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Introduction

For radical designs the hot-carrier reliability is an important issue. This creates the need for the numerical simulation of hot-carrier induced degradation. From a design point of view, the goal of the degradation simulation will be the hot-carrier aging simulation for the prediction of device lifetime. This simulation requires a complicated set of physical models, which includes the hot-carrier transport in silicon, emission process, carrier behavior in the oxide, carrier trapping, and charged interface state generation. An advanced simulation technique is also needed to obtain a self-consistent solution of the degradation under stress. Recently, several approaches are proposed [1] - [3].

This paper describes a numerical simulation of hot-carrier induced degradation under dc stress. The physical model used here and simulation results are discussed with emphasis on the degradation behavior of the buried p-MOSFET's.

Hot-Carrier Reliability of Buried p-MOSFETs

In buried p-MOSFET's, the substrate current is not a good monitor to investigate hot-carrier reliability. Fig. 1 (a) and (b) shows the substrate current I_{SUB} and the threshold voltage shift ΔV_{th} in buried p-MOSFETs with different gate-oxide thicknesses. As the gate-oxide thickness is decreased, the substrate current is increased in the wide range of the gate voltage. However, the threshold voltage shift is improved with increase of the substrate current. A significant improvement of degradation is obtained for a very thin gate oxide of 7 nm. Such correlation between I_{SUB} and ΔV_{th} is also found in the dependence of degradation on the n-well doping profile. Fig. 2 shows the threshold voltage shift versus stress gate voltage characteristics for p-MOSFETs in conventional and retrograde n-wells. The results are also compared with the measured substrate current. The substrate current for the retrograde n-well is increased by a factor of 3.0 at $V_G = -1.0$ V. There is no significant difference of degradation in the two devices. In the low stress gate voltage region ($|V_G| \leqq 1.5$ V), the device degradation for the retrograde n-well is less than that for the conventional n-well. Thus the hot-carrier reliability exhibits complicated behaviors for the fundamental scaling factors such as substrate doping profile and gate-oxide thickness.

Model of Hot-Carrier Induced Device Degradation

The degradation model is developed on the basis of the SMART-II program [4]. The model consists of the calculations of electron temperature distributions in the inhomogeneus field, emission process, carrier behavior in the oxide, and electron trapping. For surface n-MOSFET degradation, the model further requires interface state generation [5] and mobility degradation effect [6]. A self-consistent degradation model is shown in Fig. 3. In this case, the degradation behavior is calculated by an iteration of the steady-state simulations as a function of stress time. The degradation of electrical characteristics is checked at the given stress time.

The electron temperature T_n is obtained by a numerical integration along the pseudodriving force E_s.

$$T_n = T_L + \frac{2q}{5k}\int_0^\infty E_s(s-u)\,exp\,(-\frac{3u}{5\tau\cdot v_s})\,du. \qquad (1)$$

$$E_s = -\nabla\,(\psi + \frac{kT_L}{q}ln\,(n\,/\,n_i)) \qquad (2)$$

where ψ is the potential, n is the electron density. k is Boltzmann constant, and q is the electronic charge. $\tau \cdot v_s$ is 13 nm. Using the value of electron temperature, Richardson's thermal emission model further allows the calculation of injected electrons. The rate of electron trapping can be described by the equation.

$$\frac{dN(x,t)}{dt} = \frac{\sigma}{q} J_{ox}(x,t) \cdot (N_0 - N(x,t)). \quad (3)$$

where N (x, t) represents the trapped electron density at the point x. J_{ox} (x, t) is the injected electron density. σ is capture cross section, which is assumed to be 1.0×10^{-16} cm^{-2}. N_0 is the neutral trap density at t=0 taken as 1.0×10^{19} cm^{-3}. For a given stress time step Δt, the trap rate equation is written as follows:

$$N(x,t+\Delta t) = N(x,\Delta t) + (N_0 - N(x,t)) \cdot (1 - exp(-\frac{\sigma}{q} J_{ox}(x,t) \cdot \Delta t)). \quad (4)$$

The spatial distribution $N(x, t+\Delta t)$ is implemented into the device equations for the next time step. The trapped charges change the electric field in silicon and induce a channel shortening effect [7]. So, an appropriate choice of grid points in the channel is required to minimize the discretization error introduced by the stress time dependent simulation. There were 6 time steps during 10^3 seconds of stress.

Results

The model reveals the gate-oxide thickness dependence of hot-carrier induced degradation. Fig. 4 shows stress time dependence of the threshold voltage shift for 7 nm, 12 nm, and 20 nm gate-oxide devices. The thick gate oxide accelerates the degradation of the threshold voltage during stress and the 7nm gate-oxide provides a very small degradation. It is found that the hot-carrier aging simulation gives a good result for this degradation behavior. This mechanism is explained by the dynamics of the electron heating process during stress and the corresponding position of trapped electrons. The simulated spatial profiles of trapped charge are shown in Fig. 5 (a) - (c). Most of electrons in the thin gate-oxide device are trapped in the oxide above the drain region because the potential is strongly bent at the surface near the drain. The charges have little impact on the device degradation. In the case of 20 nm gate-oxide device, the trapped charge profile spreads into the direction of the channel during stress and hence the degradation is enhanced.

Moreover, the model is effective in understanding of the almost identical degradation between the p-MOSFET's in the conventional and retrograde n-wells. Fig. 6 (a) and (b) shows the potential distributions and electron densities before stress, and the electron temperature distributions along the surface during stress, for two devices, respectively. It is confirmed that there is no significant difference of stress time dependent electron energy even with high avalanche generation of electrons in the retrograde n-well. This is consistent with the experimental result of Fig. 2. As shown in the avalanched electron flow, a spill over effect of avalanched electrons [8] induces the high hot-electron resistance in the retrograde n-well.

Conclusions

A numerical simulation of hot-carrier induced degradation of buried p-MOSFET's has been demonstrated. The model allows the hot-carrier aging simulation of buried p-MOSFETs under dc stress. The gate-oxide thickness dependence of degradation and a new mechanism of hot-electron resistance in the retrograde n-well have been clarified by the numerical simulations.

Acknowledement

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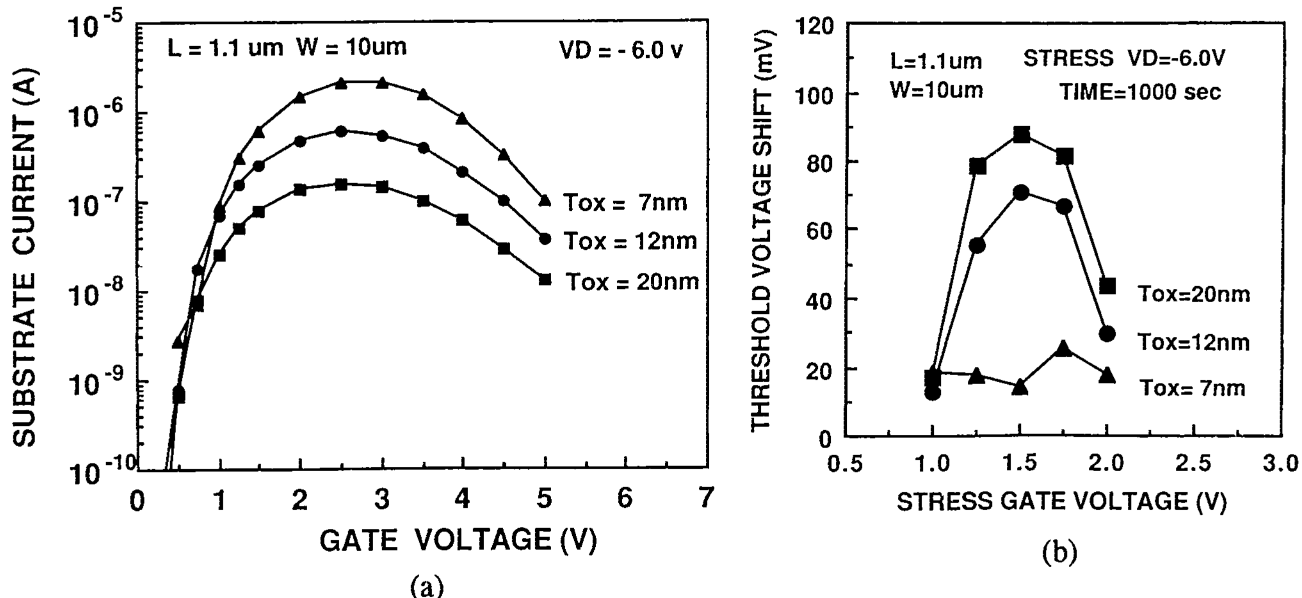

Fig. 1 (a) Substrate current and (b) threshold voltage shift for buried p-MOSFET's with 7 nm, 12 nm, and 20 nm gate-oxide thicknesses. The devices have a conventional BF_2 single drain. The effective channel length is 0.7 μm.

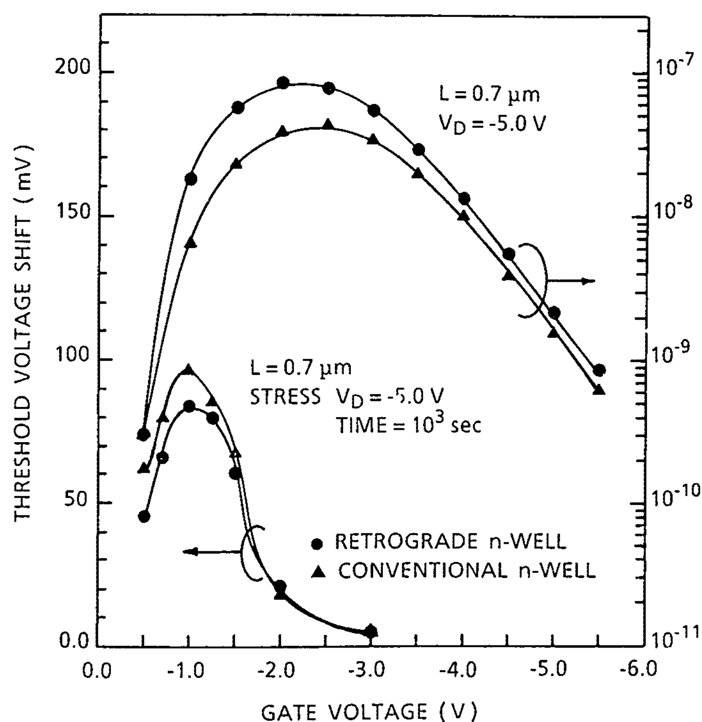

Fig. 2 Substrate current and threshold voltage shift for buried p-MOSFET's in conventional and retrograde n-wells. The devices have gate oxide thickness of 12 nm and sidewall spacers of 0.2 μm. The physical gate length is 0.7 μm.

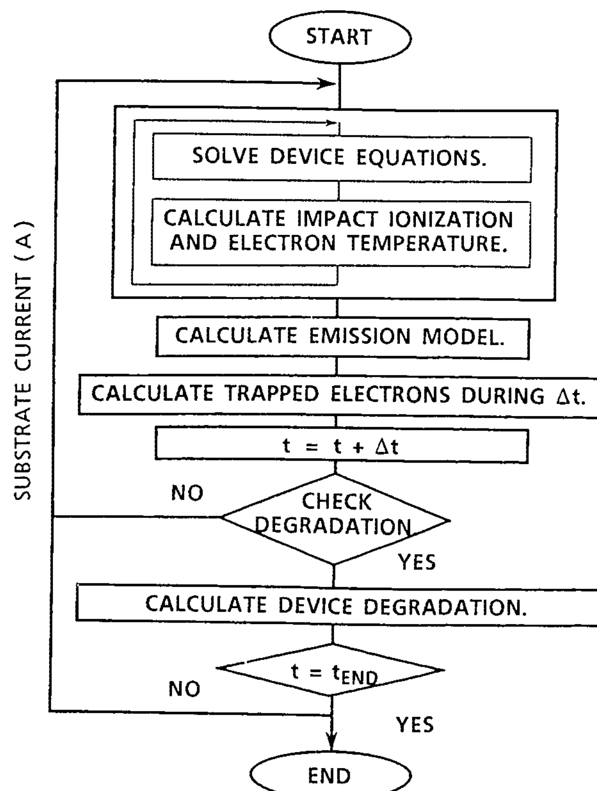

Fig. 3 Flow chart for a self-consistent degradation model.

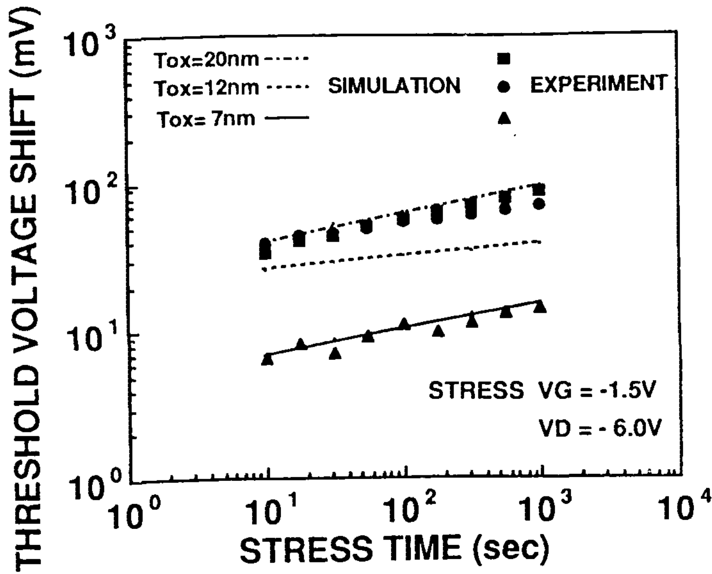

Fig. 4 Stress time dependence of the threshold voltage shift for 7 nm, 12 nm, and 20 nm gate-oxide devices. The simulations are compared with the experimental data.

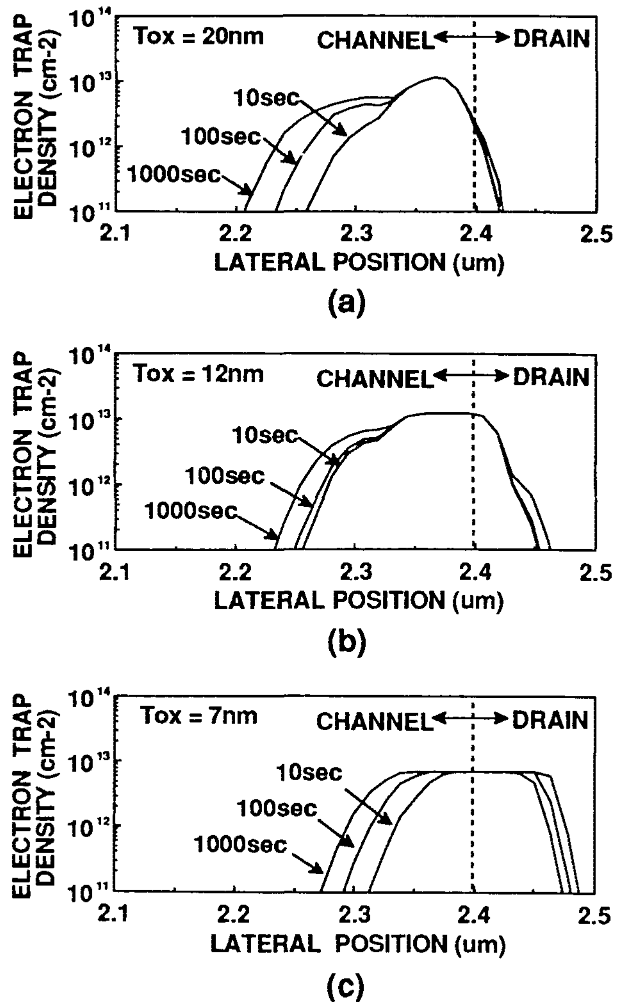

Fig. 5 Simulated spatial profiles of trapped charge. (a) 20 nm. (b) 12 nm. (c) 7 nm.

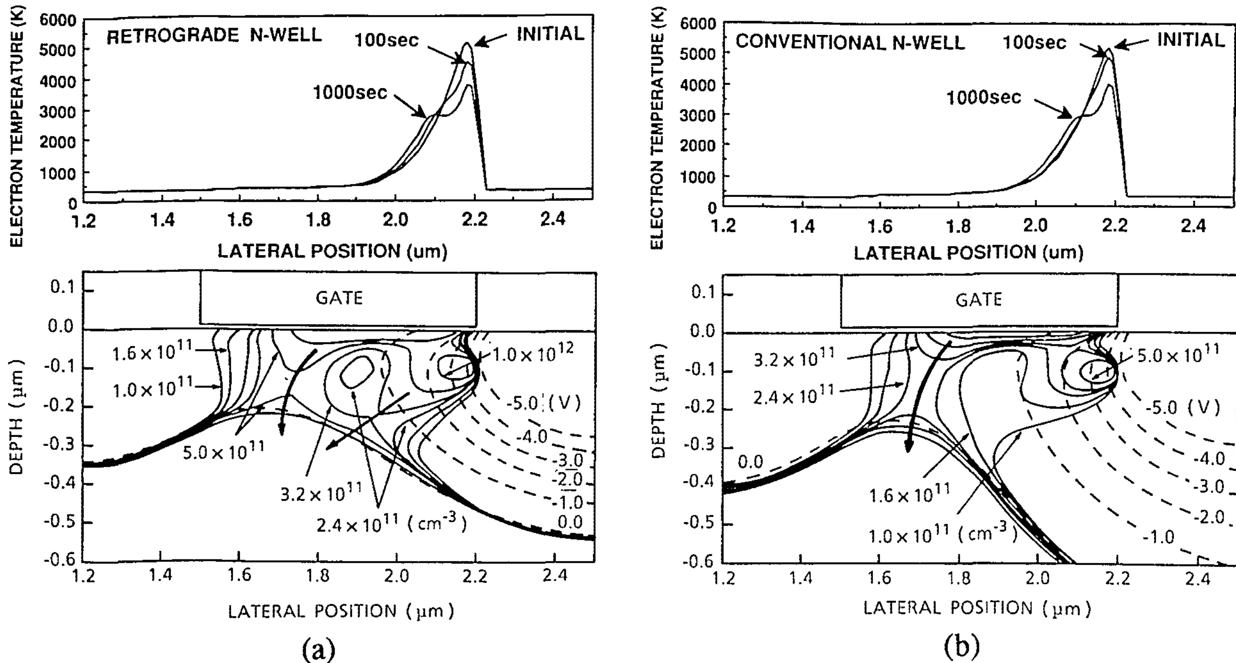

Fig. 6 Simulated results of avalanched electron distributions (solid lines), potential distributions (dashed lines), and stress time dependent electron temperature distributions. (a) Retrograde n-well. (b) Conventional n-well. The electron paths are also indicated by arrows.