CURRICULUM VITAE

Shinji Odanaka

Personal Information

Name: Shinji Odanaka

Organization: Osaka University

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Academic Background

B.S. in Applied Mathematics and Physics(1978), Kyoto University

M.S. in Applied Mathematics and Physics (1980), Kyoto University

Ph.D.in Applied Mathematics and Physics (1991), Kyoto University

Professional Experience

Professor of Cybermedia Center, Osaka University, 2000-present

Manager of ULSI Process Technology Development Center, Matsushita, 1997-2000

Project Leader of Semiconductor Research Center, Matsushita, 1985-1997

Research Staff Member of Central Research Lab, Matsushita, 1980-1985

Areas of Specialization

Numerical and mathematical modeling of semiconductor transport

Modeling and simulation of semiconductor integrated circuit processes and devices

Professional Associations

Member, Program Committee, IEEE SISPAD, 2003, 2007.

Conference Chair, IEEE SISPAD (International Conference on Simulation of Semiconductor Processes and Devices) 2002.

Member, Technical Committee, IEEE EDS, 2001-2004.

Editor, Symposium Proceedings of Material Research Society, 1999 (With H-J L.Gossmann, T.E.Hayens, M.E.Law, and A.N.Larsen).

Co-Chair, Program Committee, IEEE SISPAD, 1999.

Member, Program Committee, IEEE SISPAD, 1999-2000.

Member, Program Committee, IEEE SISPAD, 1996.
Member, Program Committee, Symposium on VLSI Technology, 1995-1999.
Member, Program Committee, NUPAD-V, 1994.
Member, Program Committee, IEEE IEDM, 1992-1993.
Member, Program Committee, NUPAD-II, 1988.
Associate Editor, IEEE Transactions on Computer-Aided Design, 1986-1988

Awards

IEEE Fellow(2007)
For contributions to numerical modeling and simulation of scaled CMOS integrated circuit processes and devices

Publications

Journal Articles

1. S.Odanaka, "A high-resolution method for quantum confinement transport simulations in MOSFETs," IEEE Transactions on CAD of ICAS, vol.26, pp.80-85, 2007.
2. S.Odanaka, "A numerical scheme for quantum hydrodynamics in a semiconductor," RIMS Kokyuroku, Kyoto University, vol.1495, pp.51-59, 2006.
3. S.Odanaka, "Multidimensional discretization of the stationary quantum drift-diffusion model for ultrasmall MOSFET structures," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.23, No.6, pp.837-842, June 2004.
4. T.Matsuda, T.Ohzone, S.Odanaka, K.Yamashita, N.Koike, and K.Tatsuuma, "A test structure for spectrum analysis of hot-carrier-induced photoemission from MOSFETs," IEEE Transactions on semiconductor Manufacturing, vol.16, pp.233-238, May 2003.
5. M. Miura-Mattausch, M.Suetake, H-J. Mattausch, S.Kumashiro, N.Shigyo, S.Odanaka, and N.Nakayama, "Physical modeling of the reverse-short-channel effects for circuit simulation", IEEE Transactions on Electron Devices, vol.48, No.10, pp.2449-2452, October 2001.
6. S.Odanaka, A.Hiroki, K. Yamashita, K.Nakanishi, and T.Noda, "Double pocket architecture using indium and boron for sub-100nm MOSFETs", IEEE Electron Device Letters, vol.22, pp.330-332, July 2001.
7. T.Noda, S.Odanaka, and H.Umimoto, "Effects of end –of range dislocation loops on

transient enhanced diffusion of indium implanted in silicon," Journal of Applied Physics, pp.4980-4984, No.9, November 2000.

8. K.Yamashita and S.Odanaka, "Interconnect scaling scenario using a chip level interconnect model," IEEE Transactions on Electron Devices, vol.47, No.1, pp.90-96, January 2000.
9. S.Odanaka, A.Misaka, and K.Yamashita, "A design hierarchy of IC interconnects and gate patterns," IEICE Transactions on Electronics, vol.E82-C,No.6, pp.948-954, June 1999.
10. T.Ohzone, T.Miyakawa, T.Matsuda, T.Yabu, and S.Odanaka, "Influence of asymmetric/symmetric source/drain region on asymmetry and mismatch of CMOSFETs and circuit performance," IEEE Transactions on Electron Devices, vol.45, February 1998.
11. S.Odanaka and A.Hiroki, "Potential design and transport property of 0.1um MOSFET with asymmetric channel profile," IEEE Transactions on Electron Devices, vol.44, pp.595-600, April 1997.
12. A.Hori, A.Hiroki, K.Moriyama-Akamatsu, and S.Odanaka, "Experimental study of impact ionization phenomena in sub-0.1um Si MOSFETs," Jpn.J.Appl.Phys. vol.35, pp.882-886, Part 1, No.2B, 1996.
13. S.Odanaka and T.Nogi, "Massively parallel computation using a splitting-up operator method for three-dimensional device simulation," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.14, pp.824-832, July 1995.
14. T.Ohzone, M.Yamamoto, H.Iwata, and S.Odanaka, "Electrical characteristics of scaled CMOSFETs with source/drain regions fabricated by 7° and 0° tilt-angle implantations," IEEE Transactions on Electron Devices, vol.42, 1995
15. T.Ohzone, H.Iwata, Y.Uraoka, and S.Odanaka, "Photon-energy distribution of hot-carrier photoemission from LOCOS- and trench-isolated MOSFETs," Solid-State Electronics, vol.37, pp.1421-1428, July 1994.
16. H.Iwata, M.Yamashita, S.Odanaka, and T.Ohzone, "Three-dimensional dynamics of heavy-ion induced CMOS latchup," IEICE Transactions on Electronics, Vol.E75-C, No.10, 1992.
17. K.Ohe, T.Yabu, S.Kugo, H.Umimoto, and S.Odanaka, "The inverse-narrow –width effect of LOCOS isolated n-MOSFET in a high-concentration p-well," IEEE Electron Devices Letters, vol.13, No.12, pp.636-638, December 1992.
18. A.Hiroki and S.Odanaka, "Gate-oxide thickness dependence of hot-carrier-induced degradation in buried p-MOSFETs", IEEE Transactions on Electron Devices,

vol.39, pp.1223-1228, May 1992.

19. S.Odanaka and A.Hiroki, “A spill over effect of avalanche-generated electrons in buried p-channel MOSFETs,” IEEE Electron Devices Letters vol.12, May 1991.
20. K.Moriyama, S.Odanaka, and Y.Ichikawa, “A three-dimensional simulation for the dynamic behavior of a trench capacitor dRAM cell,” IEICE Transactions, Vol.E 74, No.6, pp.1615-1620, June 1991.
21. H.Umimoto and S.Odanaka, “Three-dimensional numerical simulation of local oxidation of silicon,” IEEE Transactions on Electron Devices, vol.38, No.3, pp.505-511, March 1991.
22. S.Odanaka, A.Hiroki, K.Ohe, K.Moriyama, and H.Umimoto, “SMART-II:A three-dimensional CAD model for submicrometer MOSFETs,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol.10, pp.619-628, May 1991.
23. I.Nakao, H.Umimoto, S.Odanaka, T.Ohzone, and H.Esaki, “A simulation model for wet cleaning of deep trenches,” Journal of the Electrochemical Society, Vol.137, pp.2303-2305, 1990.
24. S.Odanaka, T.Yabu, N.Shimizu, H.Umimoto, and T.Ohzone, “A self-aligned retrograde twin-well structure with buried p+-layer,” IEEE Transactions on Electron Devices, vol.37, pp.1735-1742, July 1990.
25. H.Umimoto, S.Odanaka, and I.Nakao, “Numerical simulation of stress-dependent oxide growth at convex and concave corners of trench structure,” IEEE Electron Device Letters, vol.10, pp.330-332, July 1989.
26. K.Ohe, S.Odanaka, M.Moriyama, T.Hori, and G.Fuse, “Narrow-width effects of shallow trench isolated CMOS with n+-polysilicon gate,” IEEE Transactions on Electron Devices, vol.36, pp.1110-1116, June 1989.
27. S.Odanaka, T.Yabu, N.Shimizu, H.Umimoto, and T.Ohzone, “A self-aligned retrograde twin-well structure with buried p+-layer,” IEEE Electron Device Letters, vol.10, pp.280-282, June 1989.
28. A.Hiroki, S.Odanaka, K.Ohe, and H.Esaki, “A mobility model for submicrometer MOSFET simulations including hot-carrier-induced device degradation, “ IEEE Transactions on Electron Devices, vol.35, pp.1487-1493, September 1988.
29. S.Odanaka, H.Umimoto, M.Wakabayashi, and H.Esaki, “SMART-P: Rigorous three-dimensional process simulator on a super-computer,” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.7, pp.675-683, June 1988.
30. A.Hiroki, S.Odanaka, K.Ohe, and H.Esaki, “A mobility model for submicrometer

MOSFET device simulations," IEEE Electron Device Letters, vol.8, pp.231-233, May 1987.

31. G.Fuse, H.Umimoto, S.Odanaka, M.Wakabayashi, M.Fukumoto, and T.Ohzone, "Depth profiles of boron atoms with large tilt-angle implantations," J.Electrochemical Soc. vol.133, pp.996-998, May 1986.
32. S.Odanaka, M.Fukumoto, G.Fuse, M.Sasago, T.Yabu, and T.Ohzone, "A new half-micrometer p-channel MOSFET with efficient punchthrough stops," IEEE Transactions on Electron Devices vol.33, pp.317-321, March 1986.
33. S.Odanaka, M.Wakabayashi, and T.Ohzone, "The Dynamics of latchup turn-on behavior in scaled CMOS," IEEE Transactions on Electron Devices, vol.32, pp.1334-1340, July 1985.
34. S.Odanaka, M.Wakabayashi, T.Ohzone, and T.Takemoto, "A time dependent and two-dimensional device analysis of CMOS structure," Electronics & Communications in Japan Part 2: Electronics, vol.68, pp.36-43, July-August 1985.

International Conference Presentations

1. T.Shimada and S.Odanaka, "Adaptive time discretization for a transient quantum drift-diffusion model," Proceedings of SISPAD, pp.337-340,2007.
2. S.Odanaka, "Numerical approximation of the stationary quantum drif-diffusion model for multi-dimensional semiconductor devices", Workshop on Nonlinear Problems in Gauge Theory and Fluid Dynamics, Seoul, December, 2002.
3. T.Matsuda, T.Ohzone, S.Odanaka, K.Yamashita, N.Koike, and K.Tatsuuma, "A test structure for spectrum analysis of hot-carrier-induced photoemission from subquarter-micron CMOSFETs, Proceedings of ICMTS, April, 2002.
4. M.Funada, T.Matsuda, T.Ohzone, S.Odanaka, K.Yamashita, N.Koike, and K.Tatsuuma, "A new test structure to measure precise location of hot-carrier-induced photoemission peak from gate center of subquartermicron n-MOSFETs, Proceedings of ICMTS, Vol.14, pp.223-228, March, 2001.
5. K.Yamashita, S.Odanaka, K.Egashira, and T.Ueda, "On-chip interconnect evaluation on delay time increase by crosstalk," in IEDM, Digest of Technical Papers, pp.631-634, December 1999.
6. K.Nakanishi, A.Hiroki, S.Odanaka, and Y.Yamashita, "Pocket profiling of 0.1um n-MOSFETs using high dose indium implantation," Extended Abstracts of the 1999 International Conference on Solid State Devices and Materials, pp.116-117, September 1999.
7. K.Yamashita and S.Odanaka, "Impact of crosstalk on delay time and hierarchy of

interconnects," in IEDM, Digest of Technical Papers, pp.291-294, December 1998.
8. S.Ogura, A.Hori, J.Kato, M.Yamanaka, S.Odanaka, H.Fujimoto, K.Akamatsu, T.Ogura, M.Kojima, and H.Kotani, "Low voltage, low power, high speed program step split gate cell with ballistic direct injection for EEPROM/Flash," in IEDM, Digest of Technical Papers, pp.987-990, December, 1998.
9. S.Ogura, A.Hori, J.Kato, S.Odanaka, K.Akamatsu, M.Yamanaka, M.Kojima, and H.Kotani, "A novel step stack NOR cell for low voltage Flash," in Symposium on VLSI Technology, Digest of Technical Papers, pp.106-107, June 1998.
10. A.Misaka, A.Goda, S.Odanaka, S.Kobayashi, and H.Watanabe, "A statistical gate CD control including OPC," in Symposium on VLSI Technology, Digest of Technical Papers, pp.53-54, June 1998.
11. S.Odanaka, "CMOS Technology Scaling: Another prospect of scaling issues," in Proceedings, ICVC Digest of Technical Papers, pp.275-280, October 1997.
12. K.Yamashita and S.Odanaka, "Interconnect scaling scenario using a chip level interconnect model," in Symposium on VLSI Technology, Digest of Technical Papers, pp.53-54, June 1997.
13. A.Misaka, A.Goda, K.Matsuoka, H.Umimoto, and S.Odanaka, "A statistical critical dimension control at CMOS cell level," in IEDM, Digest of Technical Papers, pp.631-634, December 1996.
14. X.Wang, M.D.Giles, S.Y.Francisco, A.Leon, A.Hiroki, and S.Odanaka, "Recursive M-tree method for 3D adaptive tetrahedral mesh refinement and its application to Brillouin zone discretization," In SISPAD, Digests of Technical Papers, pp.67-68, 1996.
15. K.Eriguchi, Y.Uraoka, and S.Odanaka, "A new gate oxide lifetime prediction method using cumulative damage law and its application to plasma-damaged oxides," in IEDM, Digest of Technical Papers, pp.323-326, December 1995.
16. A.Hiroki, S.Odanaka, and A.Hori, "A high performance 0.1um MOSFET with asymmetric channel profile," in IEDM, Digest of Technical Papers, pp.439-442, December 1995.
17. S.Odanaka, H.Umimoto, A.Hiroki, K.Kurimoto, A.Misaka, K.Akamatsu, "TCAD: Challenges to virtual process," in Proceedings, ICVC Digest of Technical Papers, pp.197-202, October 1995.
18. H.Umimoto, S.Odanaka, and A.Goda, "A three-dimensional process simulation using advanced SMART-P program," in SISDEP, Digest of Technical Papers, pp.30-56, September 1995.
19. K.Yamashita, H.Nakaoka, K.Kurimoto, H.Umimoto, and S.Odanaka, "Impact of the

reduction of the gate to overlapped CMOS devices," In Symposium on VLSI Technology, Digest of Technical Papers, pp.69-70, 1995.

20. A.Hori, H.Nakaoka, H.Umimoto, K.Yamashita, M.Takase, N.Shimizu, B.Mizuno, and S.Odanaka, "A 0.05 μ m-CMOS with ultra shallow source/drain junctions fabricated by 5keV ion implantation and rapid thermal annealing," in IEDM, digest of Technical Papers, pp.485-488, December 1994.
21. K.Kurimoto, K.Yamashita, I.Miyanaga, A.Hori, and S.Odanaka, "An electrothermal circuit simulation using an equivalent thermal network for electrostatic charge(ESD)," in Symposium on VLSI Technology, Digest of Technical Papers, pp.127-128, June 1994.
22. A.Hiroki, S.Odanaka, and A.Goda, "Massively parallel computation for Monte carlo device simulation," Proceedings of VPAD, pp.18-19, May 1993.
23. T.Ohzone, H.Iwata, Y.Uraoka, and S.Odanaka, "A two-dimensional analysis of hot-carrier photoemission from LOCOS- and trench-isolated MOSFETs," in IEDM, Digest of technical Papers, pp.527-530, December 1992.
24. H.Umimoto, S.Odanaka, and S.Imai, "A 3D BPSG flow simulation with temperature and impurity concentration dependent viscosity model," in IEDM, Digest of technical Papers, pp.709-712, December 1991.
25. K.Kurimoto and S.Odanaka, "A T-gate overlapped LDD device with high circuit performance and high reliability," in IEDM, Digest of Technical Papers, pp.541-543, December 1991.
26. H.Umimoto, S.Odanaka, and S.Imai, "A three-dimensional dynamic simulation of boronphosphosilicate glass flow," in Symposium on VLSI Technology, Digest of Technical Papers, pp.99-100, May 1991
27. S.Odanaka and A.Hiroki, "A numerical simulation of hot-carrier induced device degradation," in International Workshop on VLSI Process/Device Modeling(VPAD), Technical Digest, pp.108-111, May 1991.
28. S.Odanaka and A.Hiroki, "Gate-oxide thickness dependence of hot-carrier-induced degradation in buried p-MOSFET," in IEDM, pp.565-568, December 1990.
29. H.Umimoto and S.Odanaka, "Multi-dimensional numerical modeling for thermal oxidation of silicon," Proceedings of the 1st International Conference and Exhibition on Computer Applications to Materials Science and Engineering-CAMSE, pp.729-734, 1990.
30. Y.Odake, K.Kurimoto, and S.Odanaka, "Three-dimensional numerical modeling of the indirect band-to-band tunneling in MOSFETs," Extended Abstracts of the 22th Conference on Solid State Devices and materials, pp.131-134, August 1990.

31. S.Odanaka, K.Zaiki, and T.Nogi, “Three-dimensional device simulation on a super-parallel computer : ADENA,” in International Workshop on VLSI Process/Device Modeling, Technical Digest, pp.122-125, August 1990.
32. K.Kurimoto, Y.Odake, and S.Odanaka, “Drain leakage current characteristics due to the band-to-band tunneling in LDD MOS devices,” in IEDM, Digest of Technical Papers, pp.621-624, December 1989.
33. S.Odanaka, A.Hiroki, K.Ohe, H.Umimoto, and K.Moriyama, “SMART-II : A three-dimensional CAD model for submicrometer MOSFETs,” Proc.NASECODE VI Conference pp.303-310, Doublin:Boole Press, July 1989.
34. T.Yabu, S.Odanaka, H.Umimoto, N.Shimizu, and T.Ohzone, “An advanced half-micrometer CMOS device with self-aligned retrogarade twin-wells and buried p+-layer,” in Symposium on VLSI Technology, Digest of Technical Papers, pp.35-36, May 1989.
35. H.Umimoto and S.Odanaka, “Three-dimensional simulation of local oxidation of silicon,” in Symposium on VLSI Technology, Digest of Technical Papers, pp.47-48, May 1989.
36. A.Hiroki and S.Odanaka, “Physical modeling of MOSFET degradation induced by high-energy hot carriers,” Extended Abstracts of the 20th Conference on Solid State Devices and Materials, pp.221-224, August 1988.
37. H.Umimoto, S.Odanaka, and I.Nakao, “Simulation of stress-dependent oxide growth at the convex and concave corners of trench structures,” in Symposium on VLSI Technology, Digest of Technical Papers, pp.47-48, May 1988.
38. G.Fuse, H.Ogawa, K.Tateiwa, I.Nakao, S.Odanaka, M.Fukumoto, H.Iwasaki, and T.Ohzone, “A practical trench isolation technology with a novel planalization process,” In IEDM, Digest of Technical Papers, pp.732-735, December 1987.
39. S.Odanaka, M.Wakabayashi, H.Umimoto, A.Hiroki, K.Ohe, K.Moriyama, H.Iwasaki, and H.Esaki, “SMART : Three-dimensional process/device simulator integrated on a super-computer,” in Proceedings, International Symposium on Circuits and Systems, pp.534-537, May 1987.
40. S.Odanaka, H.Umimoto, M.Wakabayashi, and H.Esaki, “Rigorous three-dimensional process simulator on a super-computer : SMART-P,” in ICCAD-86, Digest of Technical Papers, pp.468-471, November 1986.
41. G.Fuse, S.Odanaka, M.Sasago, M.Fukumoto, A.Shinohara, H.Umimoto, T.Yabu, T.Ohzone, and T.Ishihara, “Trench isolation with boron implanted side-walls for controlling narrow-width effect of n-MOS threshold voltages,” in Symposium on VLSI Technology, Digest of Technical Papers, pp.58-59, May 1985.

42. S.Odanaka, M.Fukumoto, G.Fuse, A.Shinohara, M.Sasago, T.Yabu, T.Ohzone, and T.Ishihara, “A new half-micron p-channel MOSFET with efficient punchthrough stops,” in Symposium on VLSI Technology, Digest of Technical Papers, pp.62-63, May 1985.